FIG. 1

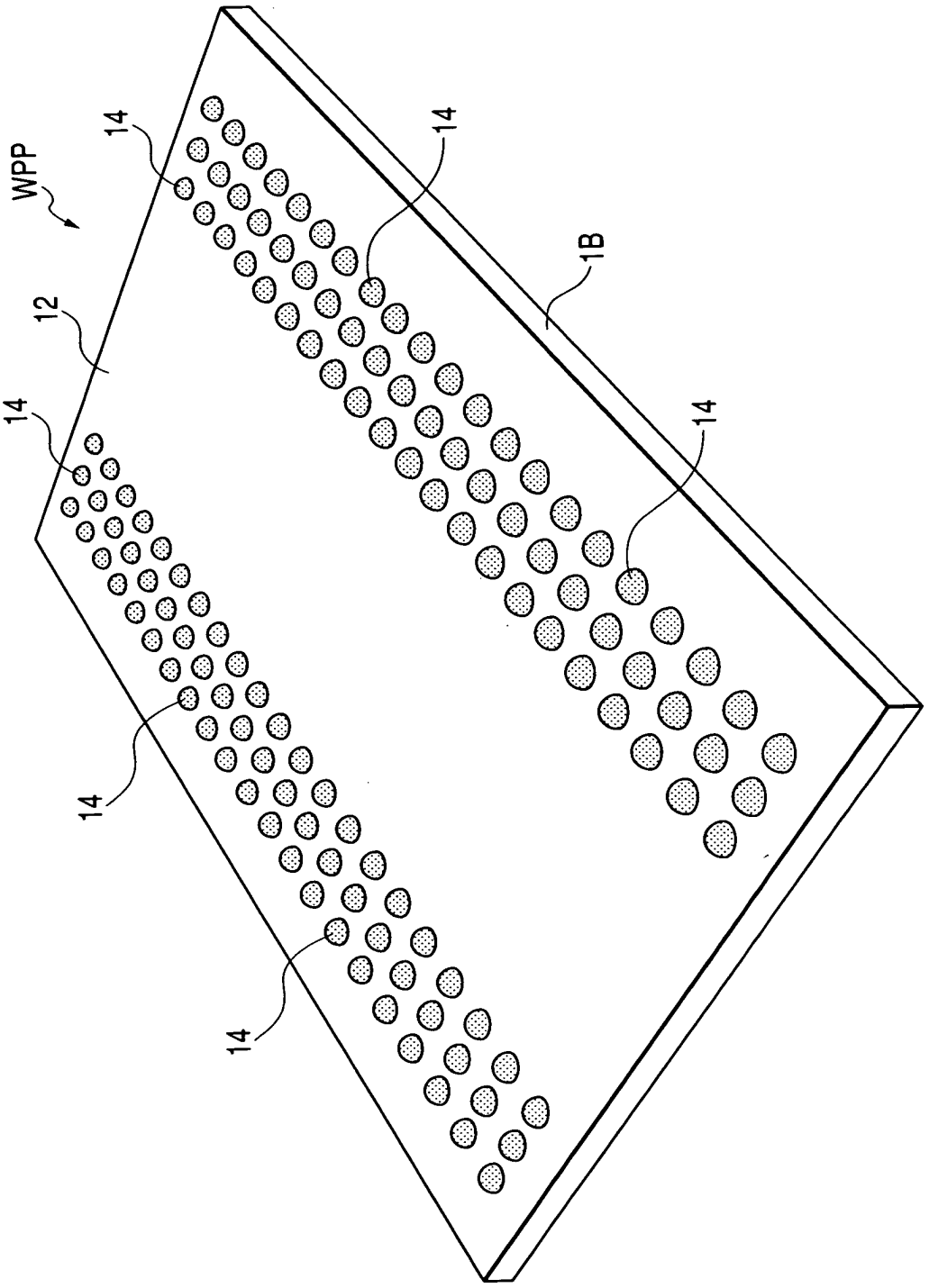


FIG. 2

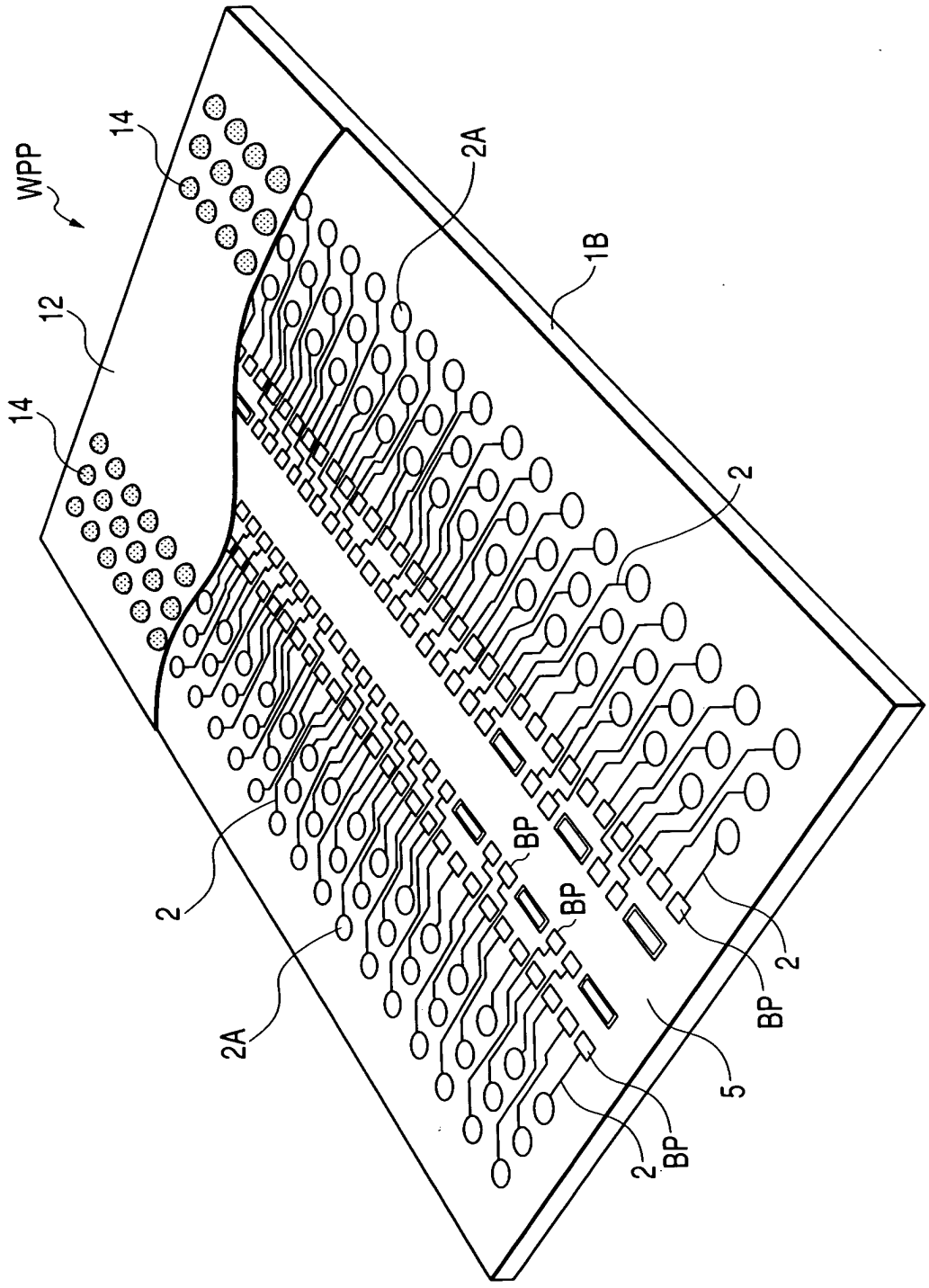


FIG. 3

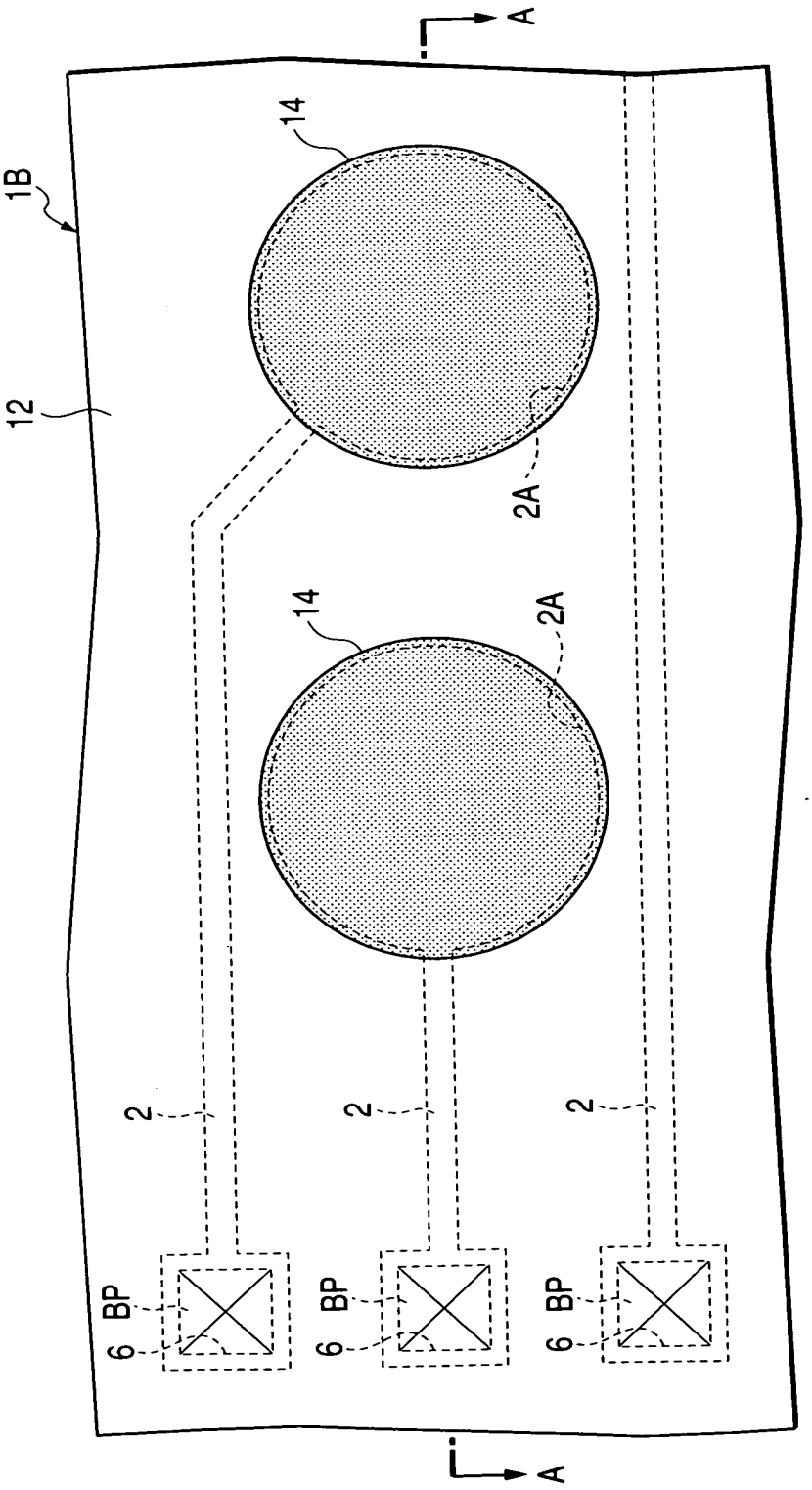


FIG. 4

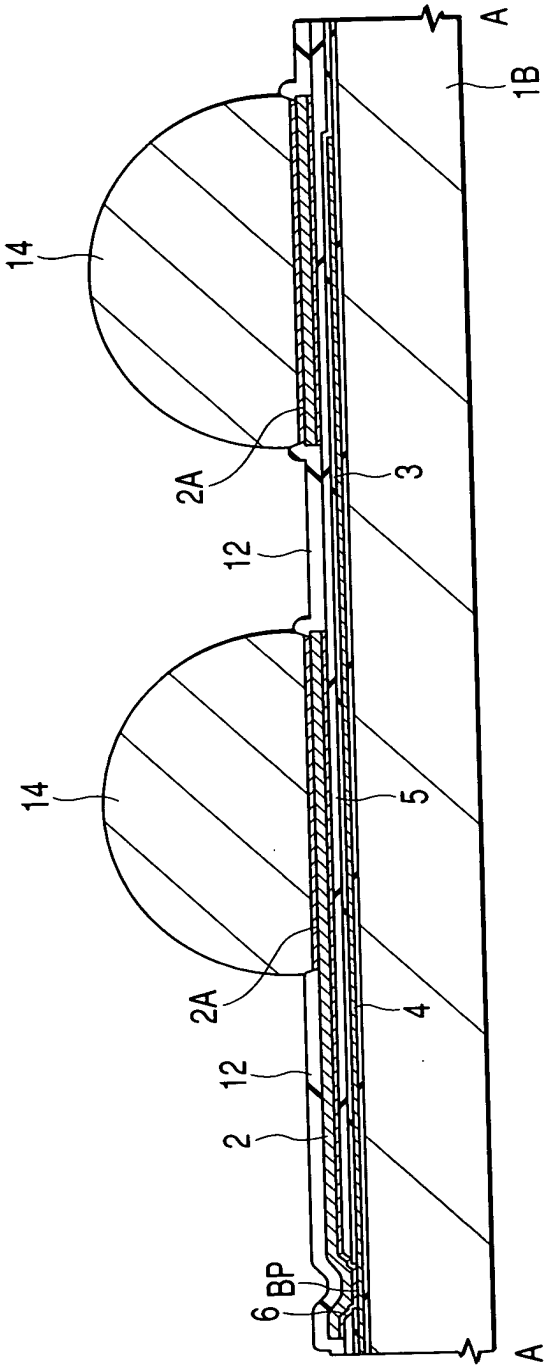
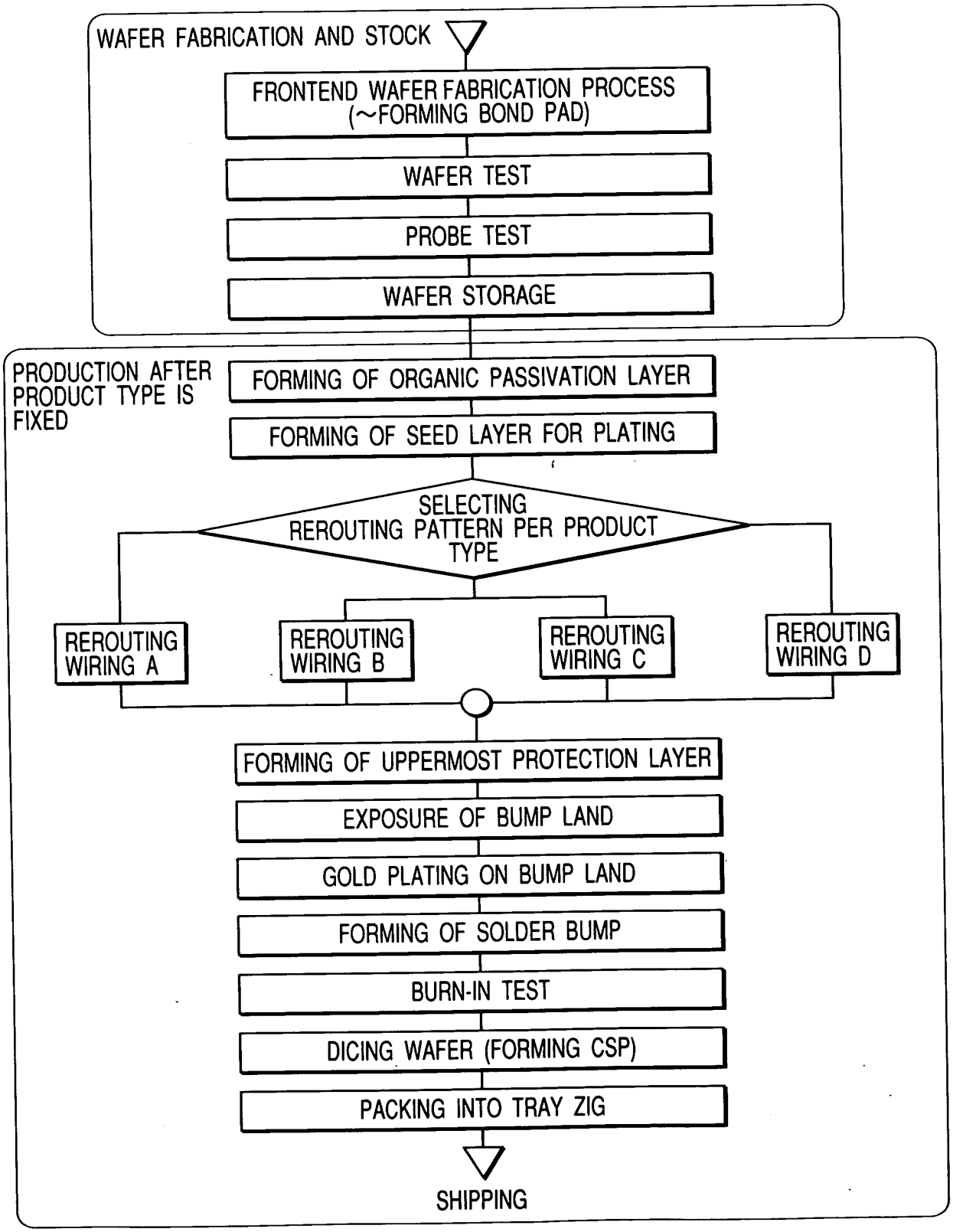


FIG. 5


WAFER FABRICATION AND STOCK
FRONTEND WAFER FABRICATION PROCESS (~FORMING BOND PAD)
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PROBE TEST
WAFER STORAGE
PRODUCTION AFTER PRODUCT TYPE IS FIXED
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REROUTING WIRING D
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GOLD PLATING ON BUMP LAND
FORMING OF SOLDER BUMP
BURN-IN TEST
DICING WAFER (FORMING CSP)
PACKING INTO TRAY ZIG
SHIPPING

FIG. 6

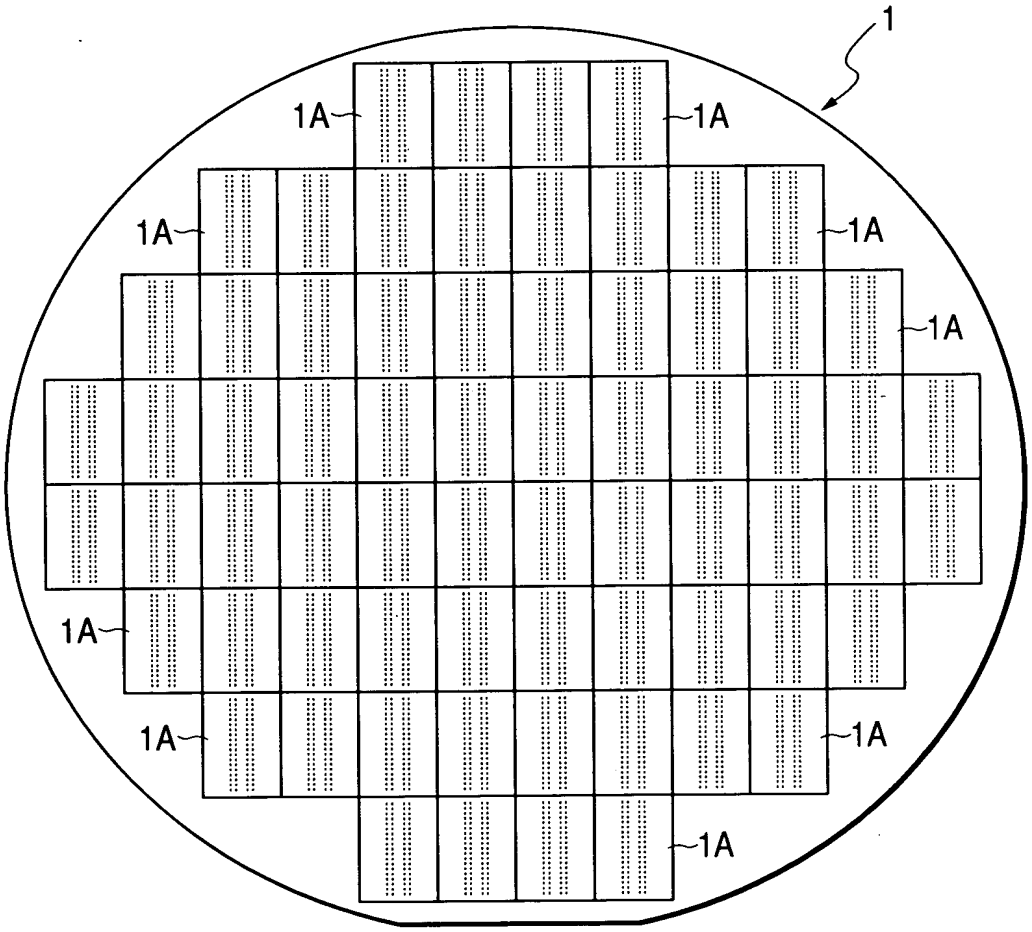


FIG. 7

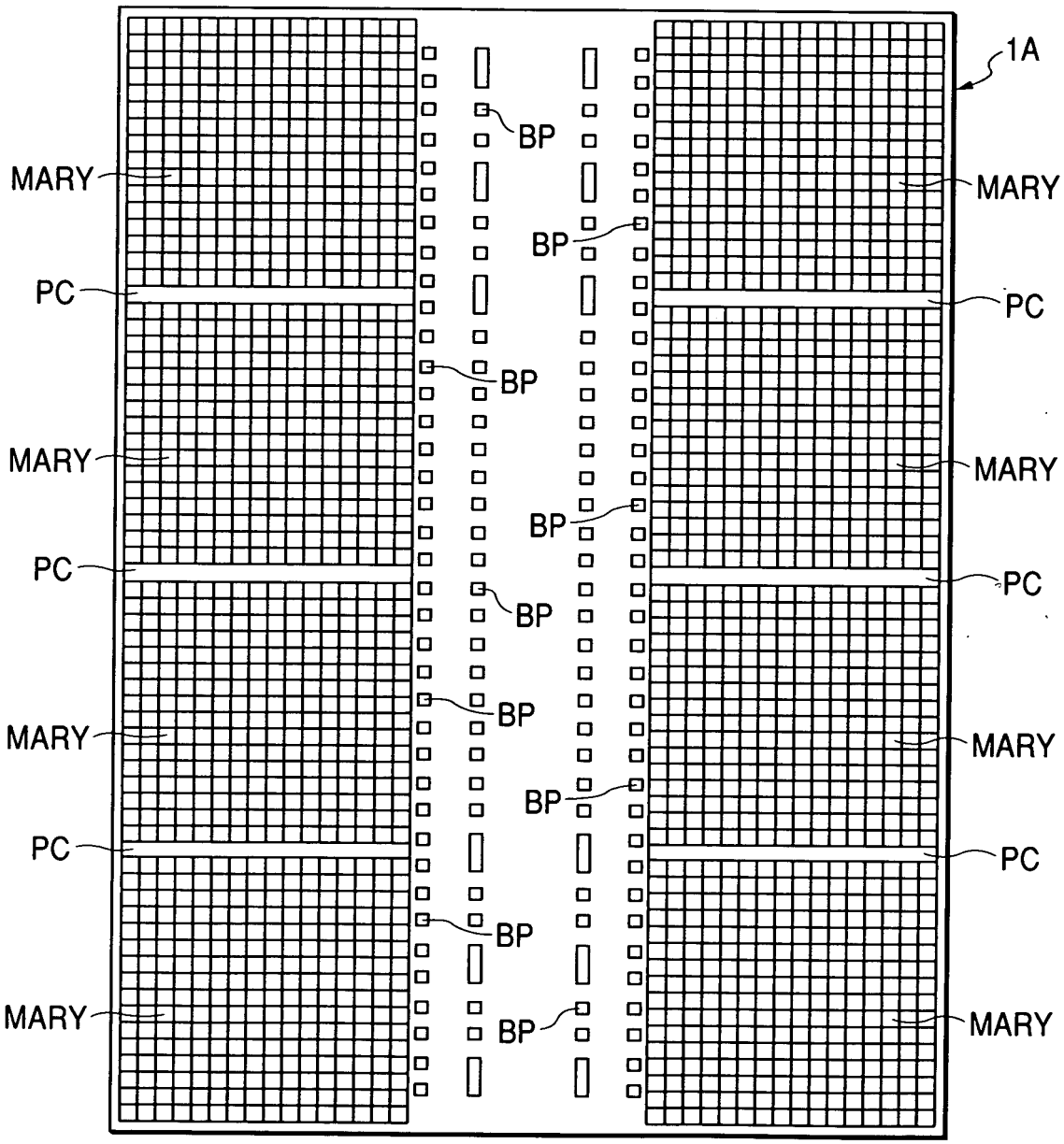


FIG. 8

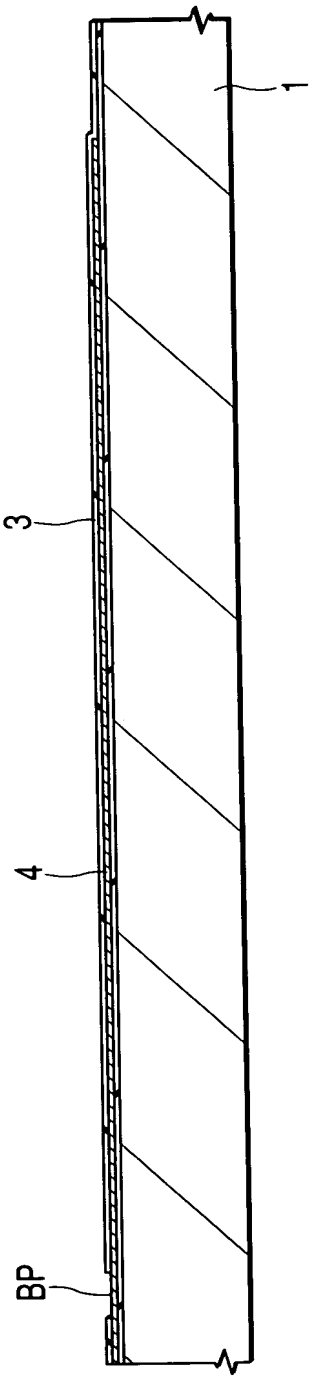


FIG. 9

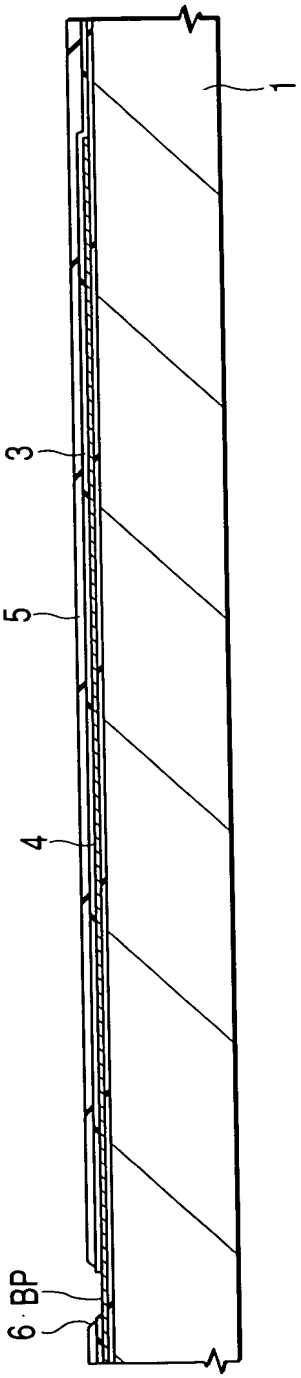


FIG. 10

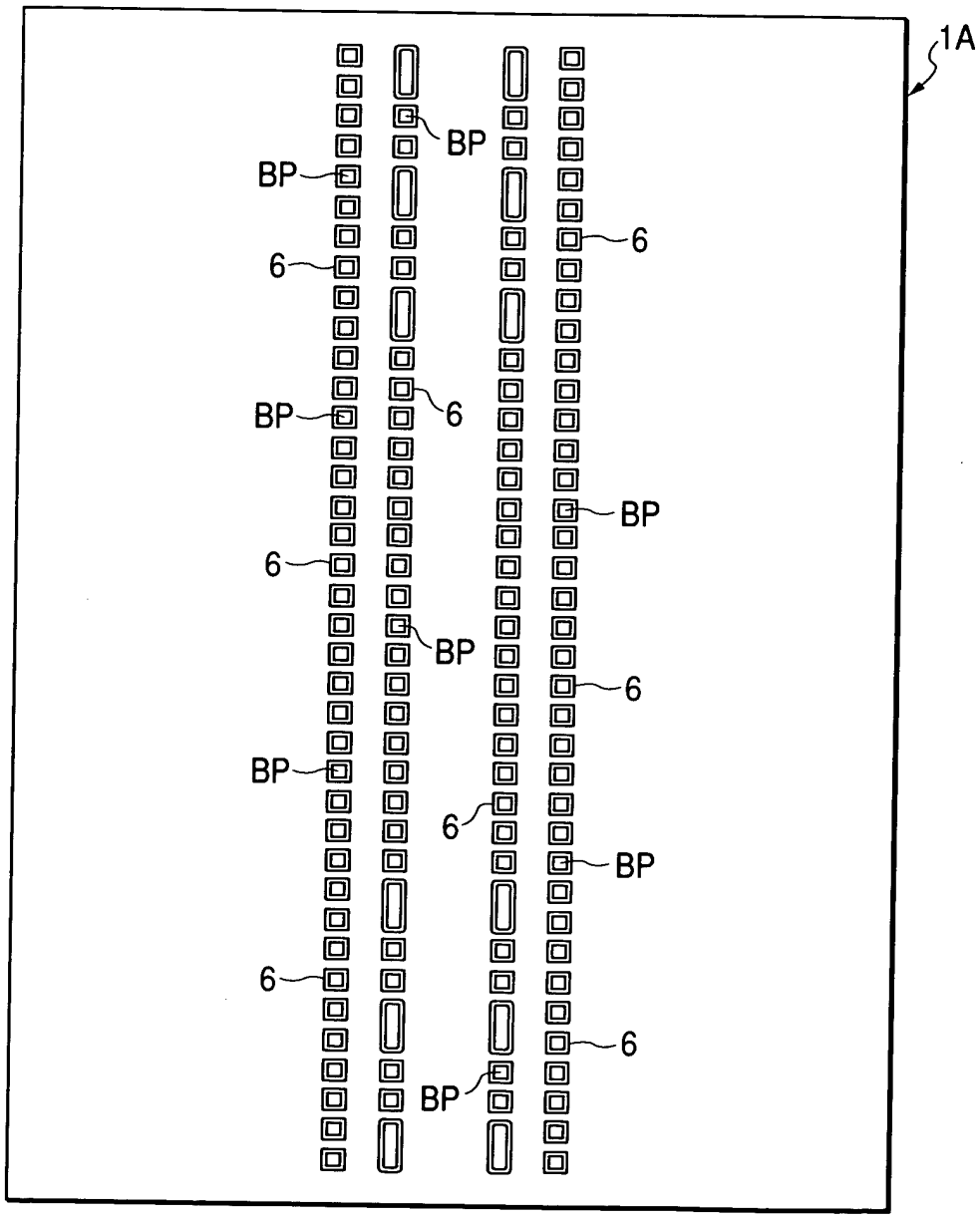


FIG. 11

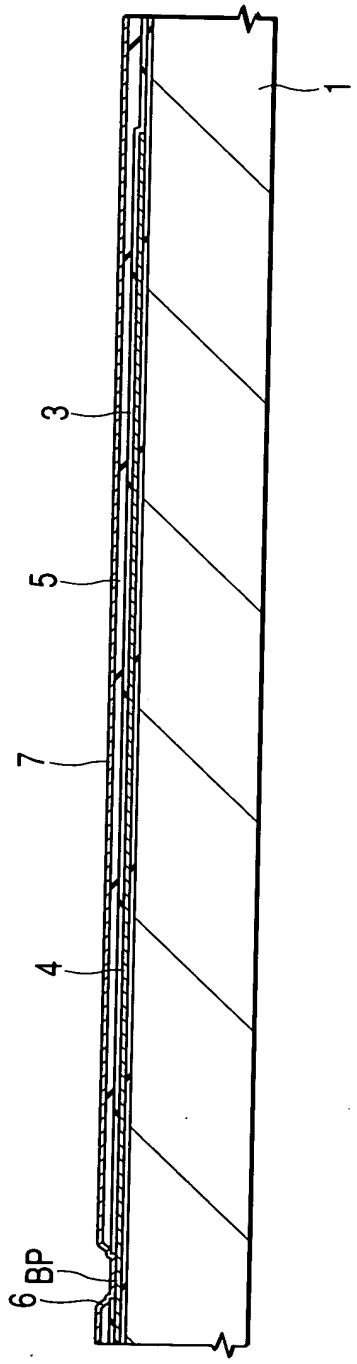


FIG. 12

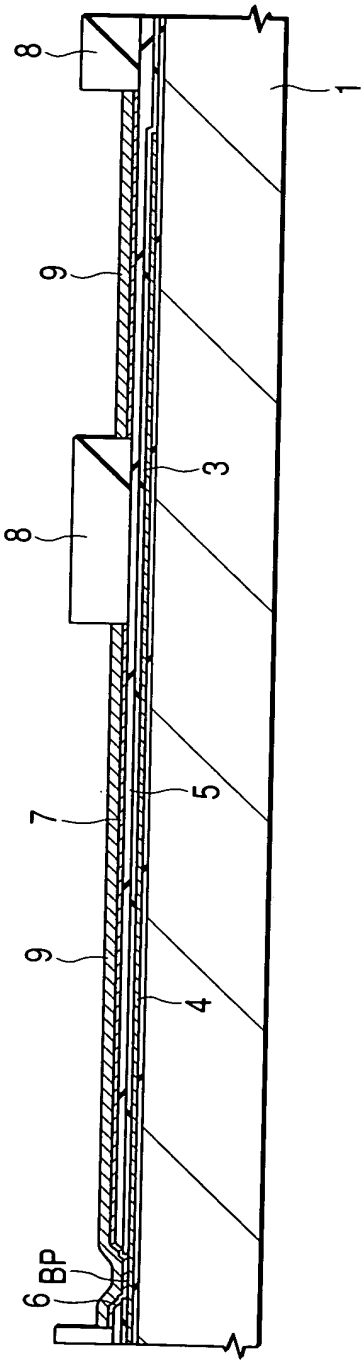


FIG. 13

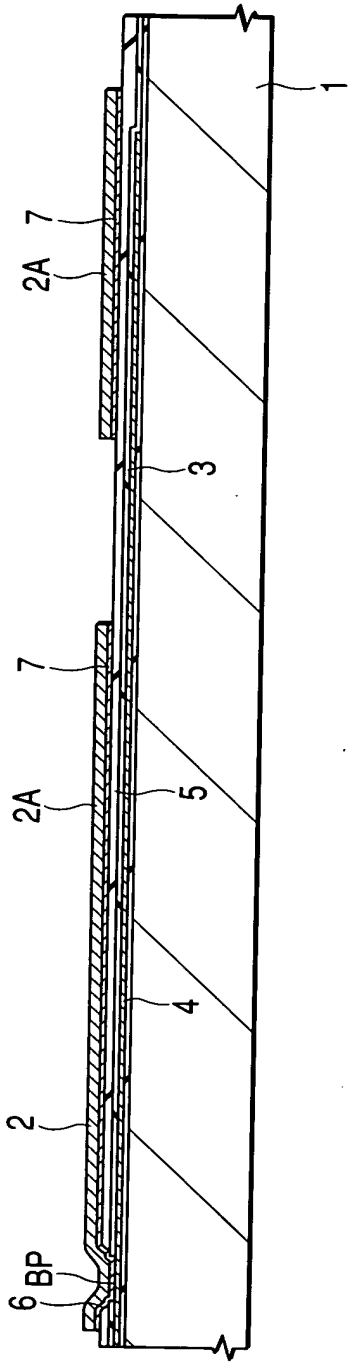


FIG. 14

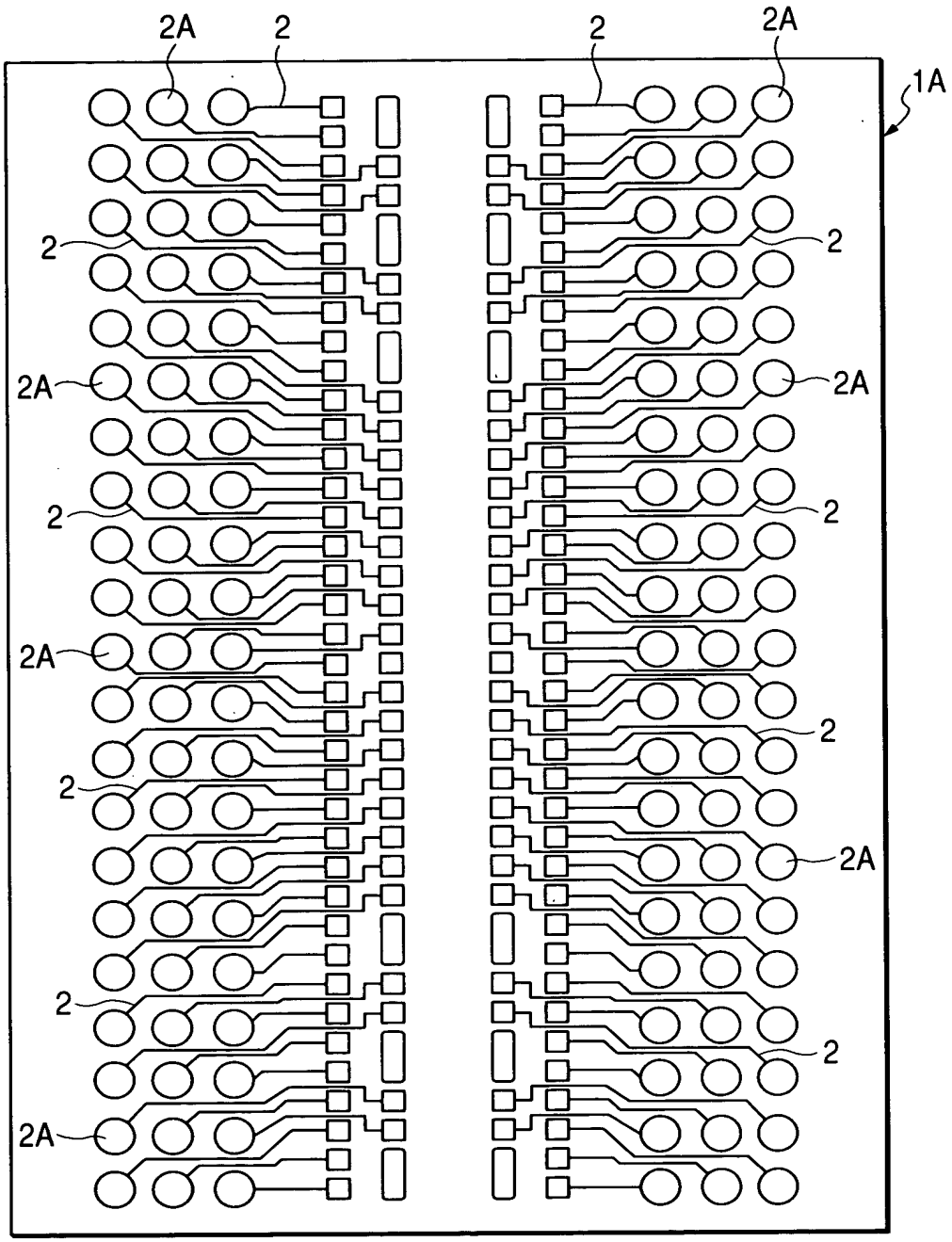


FIG. 15(a)

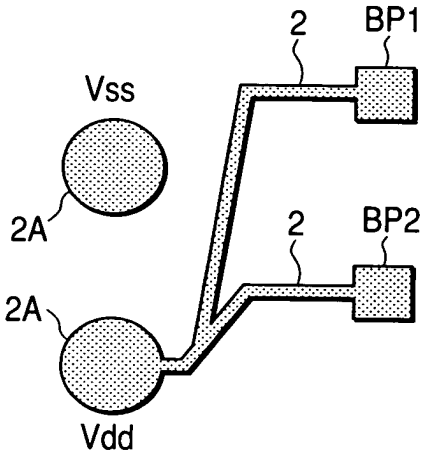


FIG. 15(c)

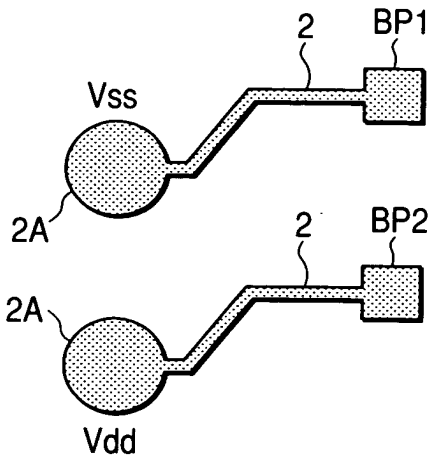


FIG. 15(b)

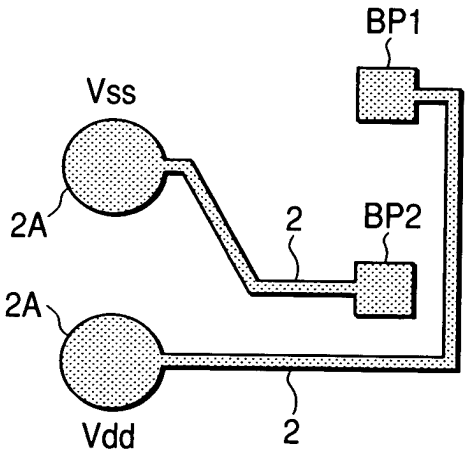


FIG. 15(d)

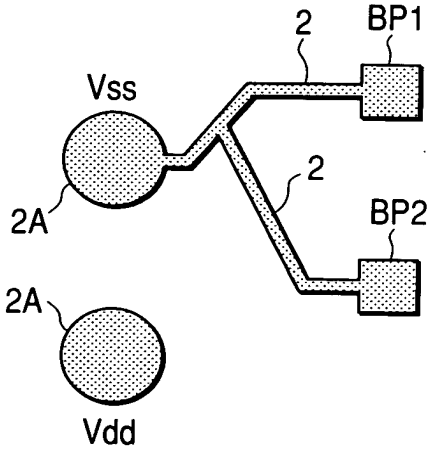


FIG. 16

FUNCTION	PAD		BIT STRUCTURE	ACTION MODE	
	BP1	BP2		DDR	SYNCHRONOUS
FUNCTION 1	Vdd	Vdd	×32Bit	○	—
FUNCTION 2	Vdd	Vss	×32Bit	—	○
FUNCTION 3	Vss	Vdd	×64Bit	○	—
FUNCTION 4	Vss	Vss	×64Bit	—	○

FIG. 17

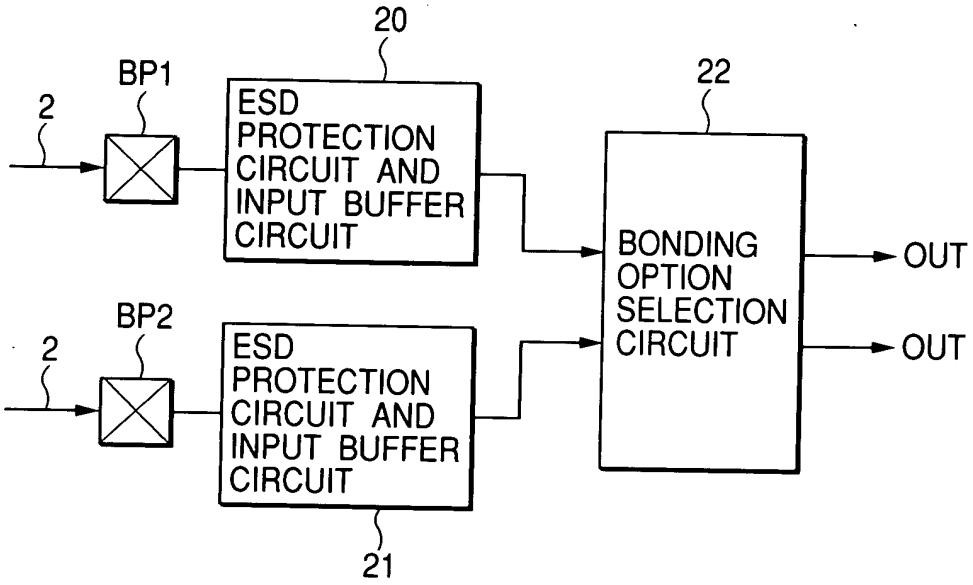


FIG. 18(a)

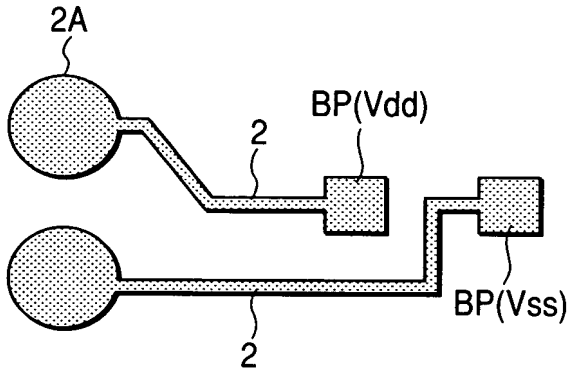


FIG. 18(b)

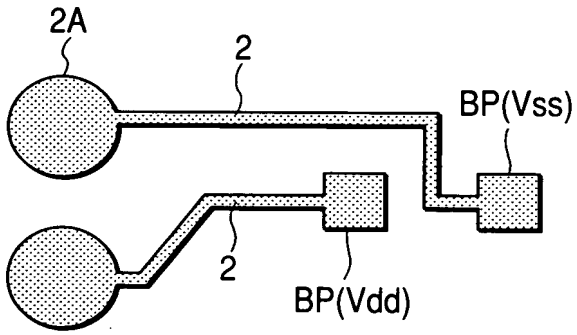


FIG. 19

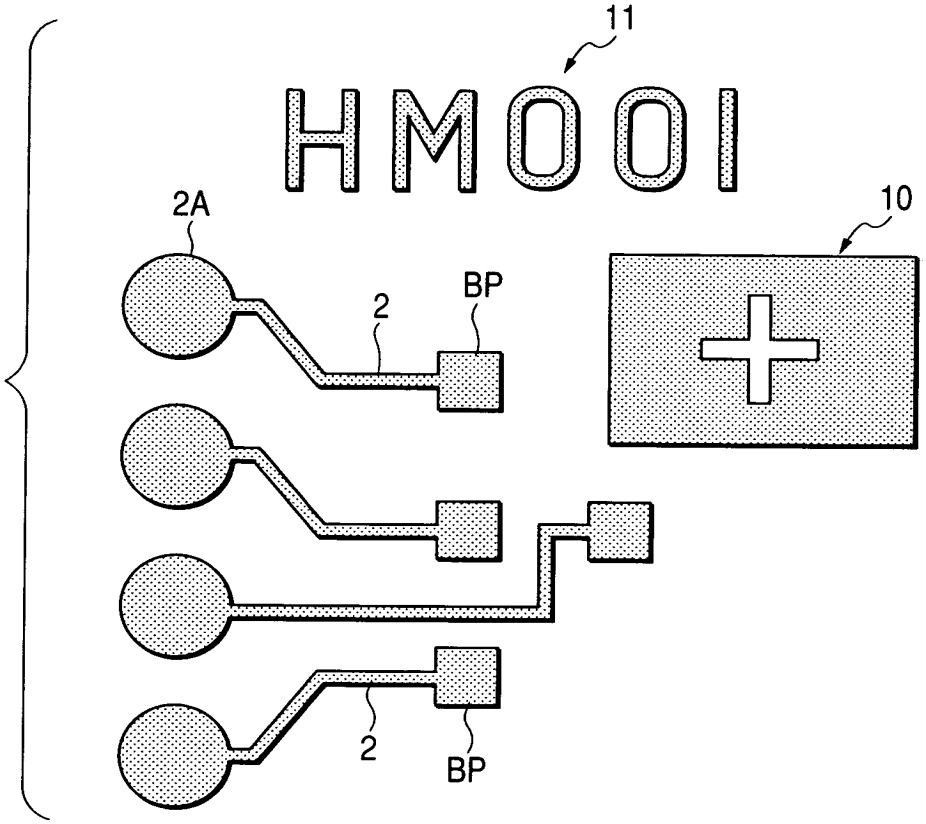


FIG. 20

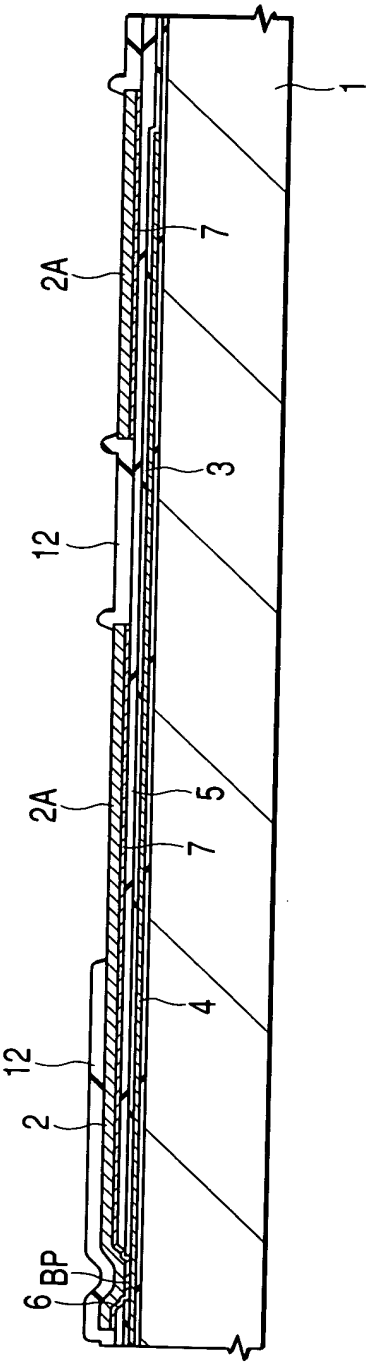


FIG. 21

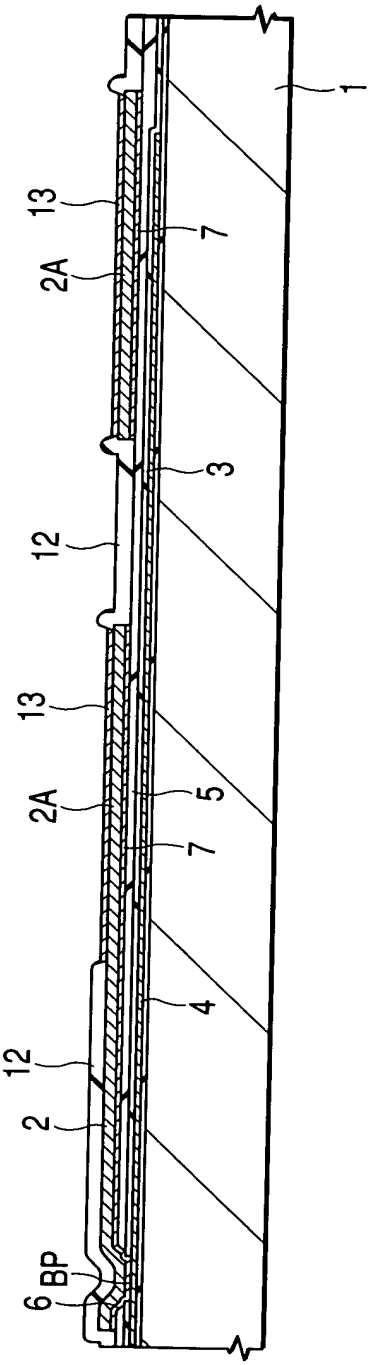


FIG. 22

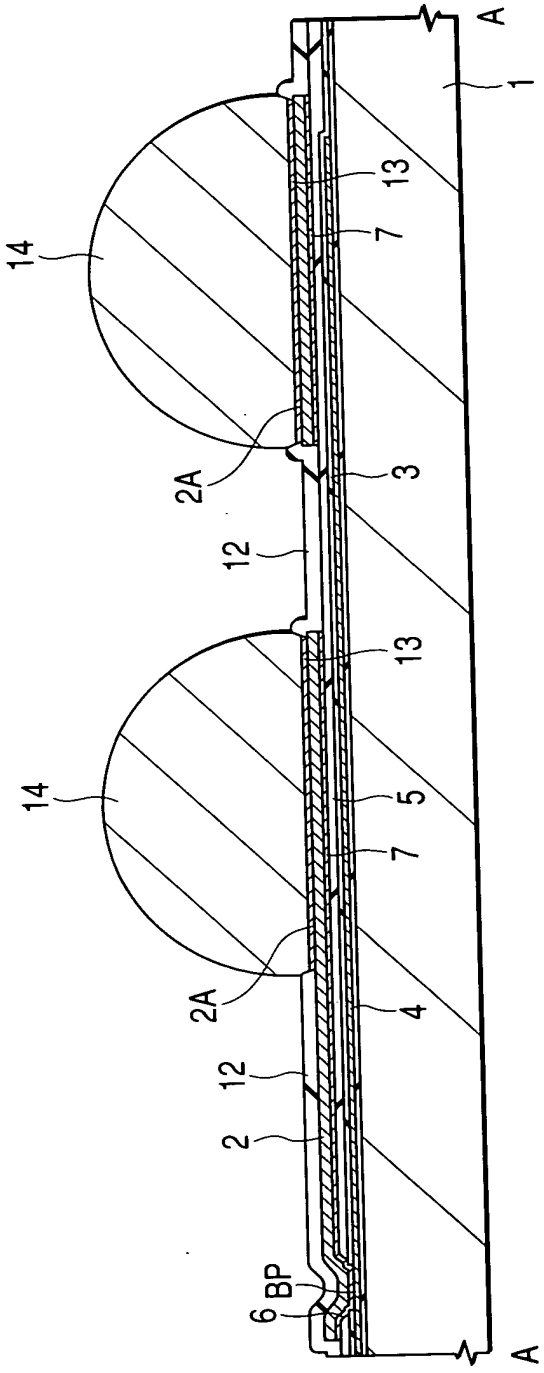


FIG. 23

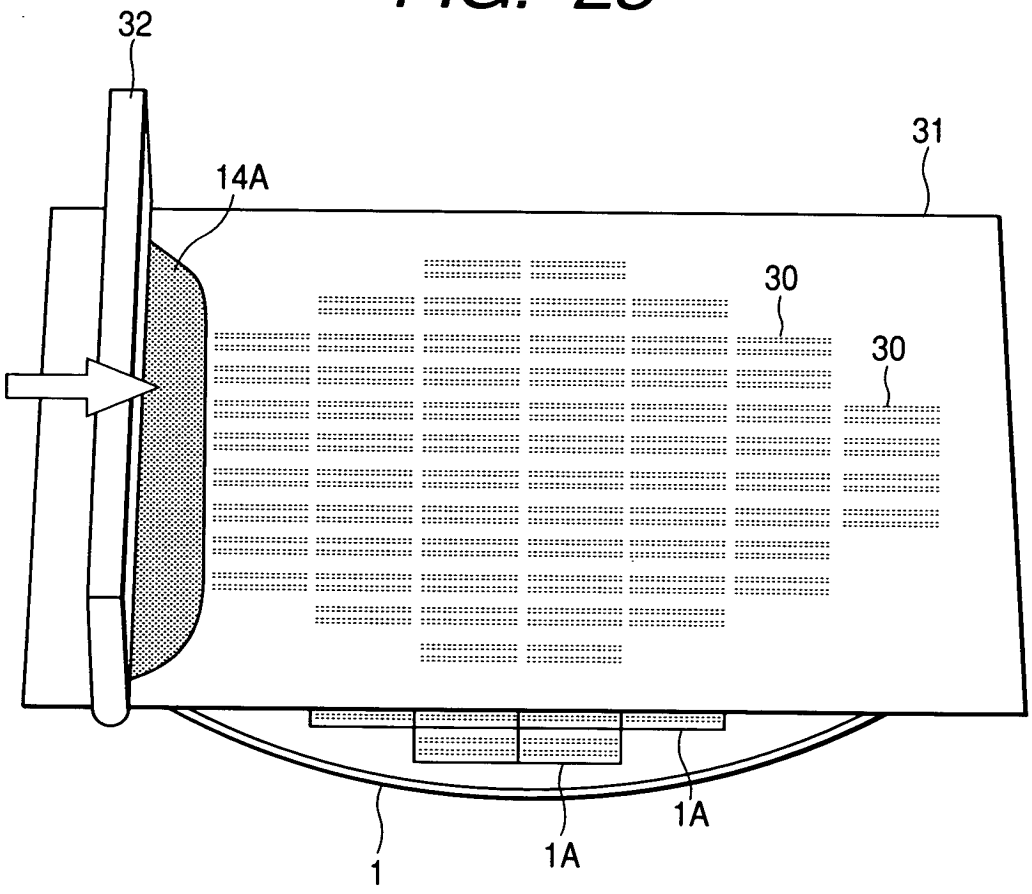


FIG. 24

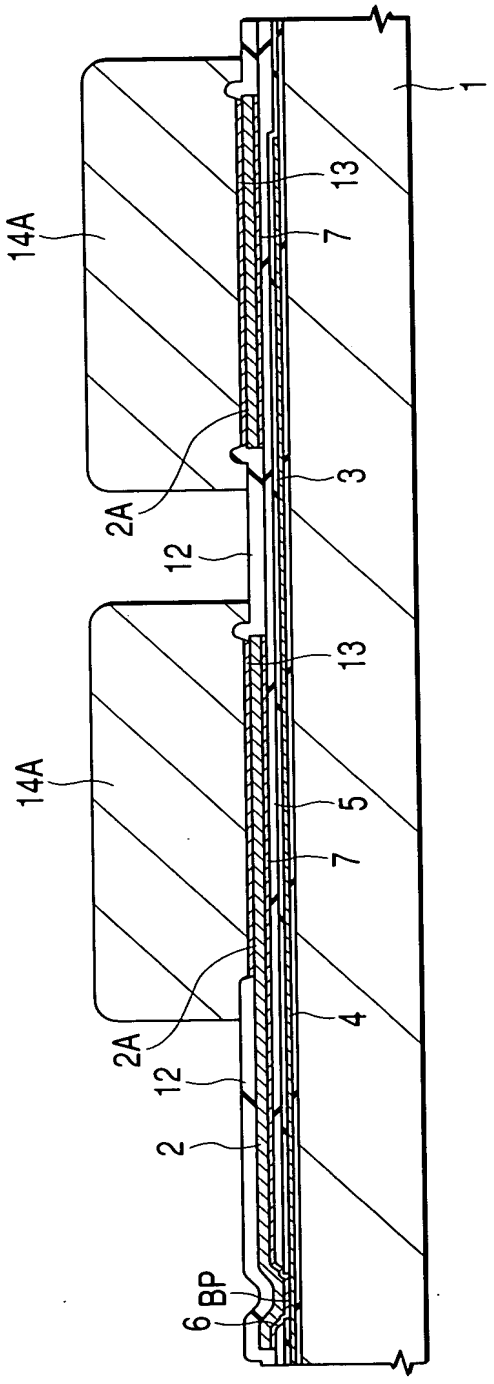


FIG. 25

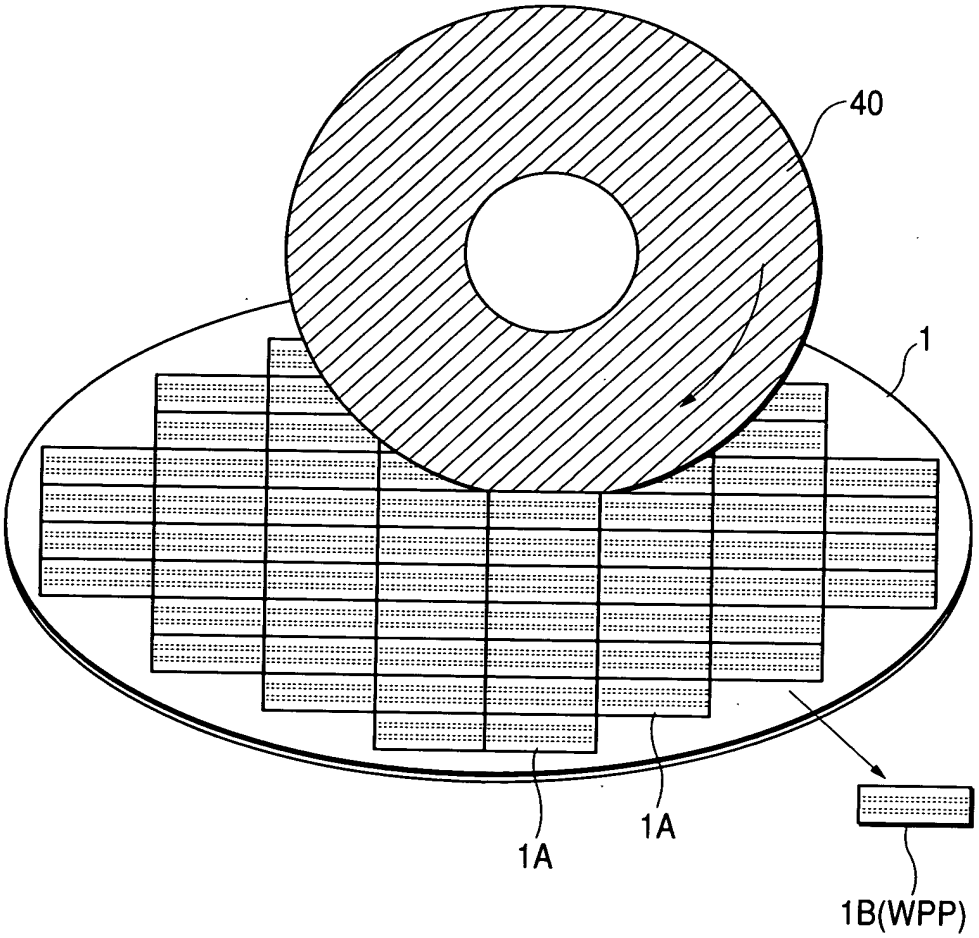
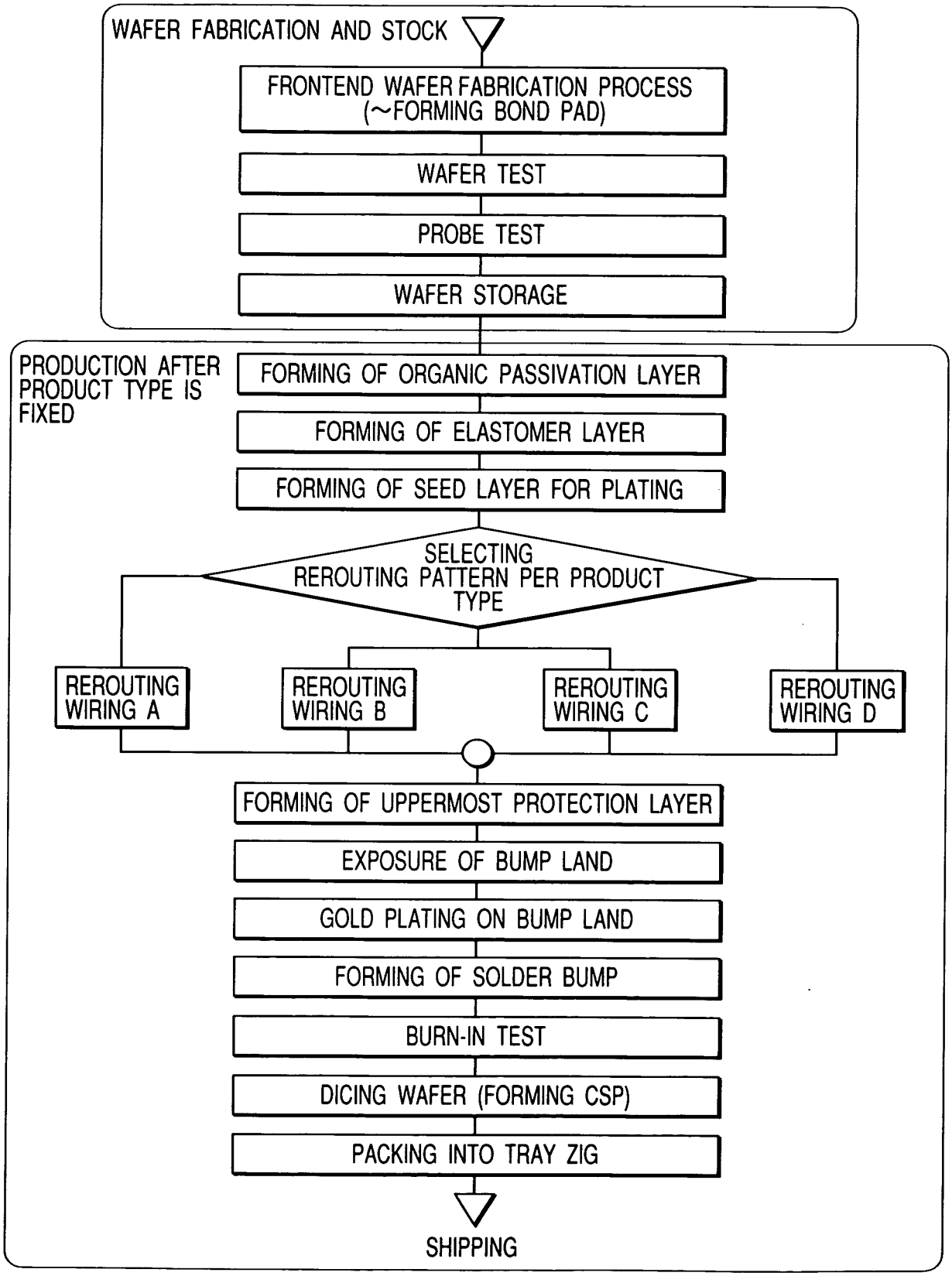


FIG. 26


WAFER FABRICATION AND STOCK
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PROBE TEST
WAFER STORAGE
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FORMING OF SOLDER BUMP
BURN-IN TEST
DICING WAFER (FORMING CSP)
PACKING INTO TRAY ZIG
SHIPPING

FIG. 27

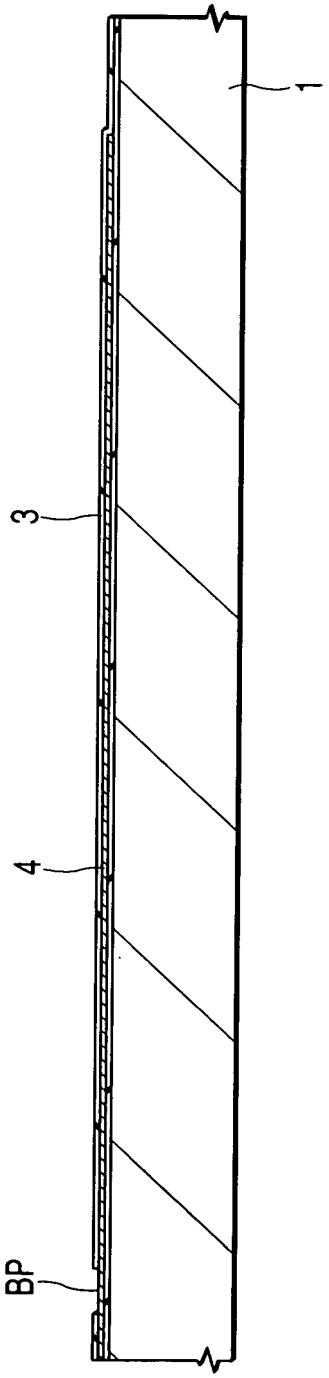


FIG. 28

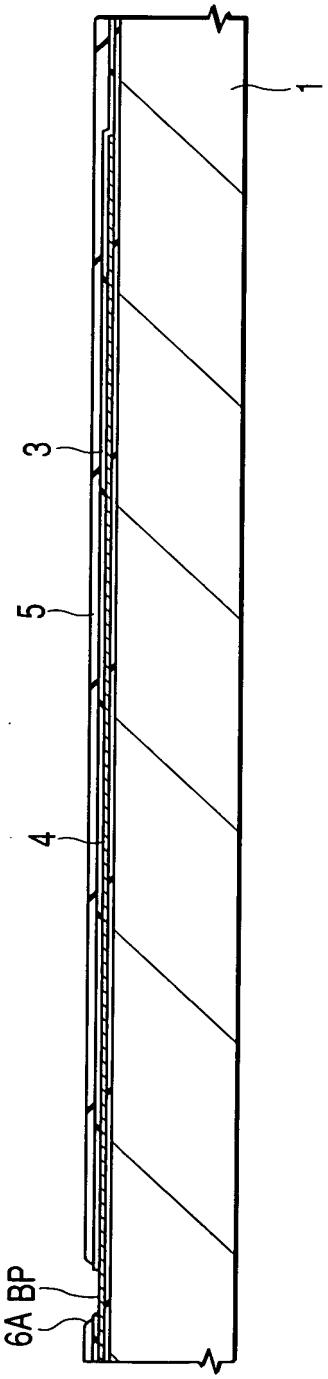


FIG. 29

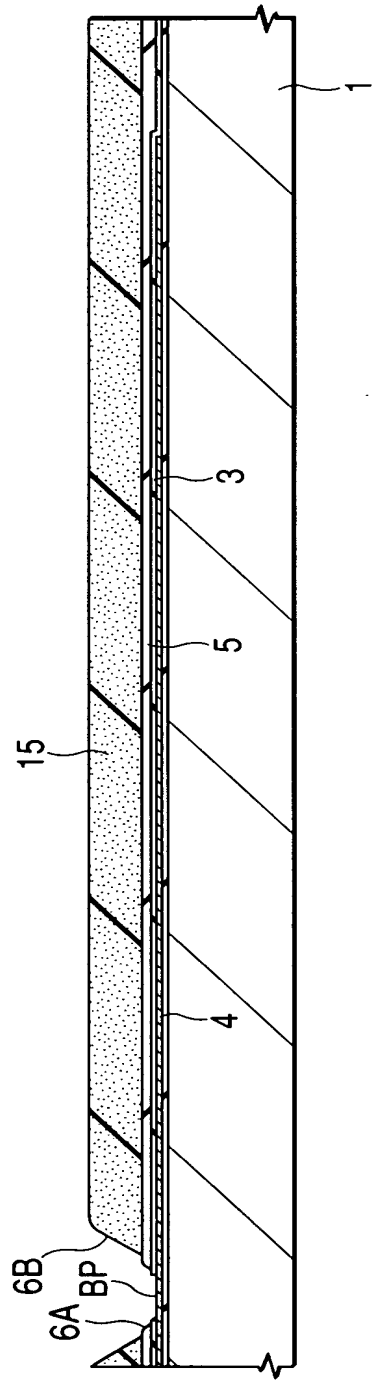


FIG. 30

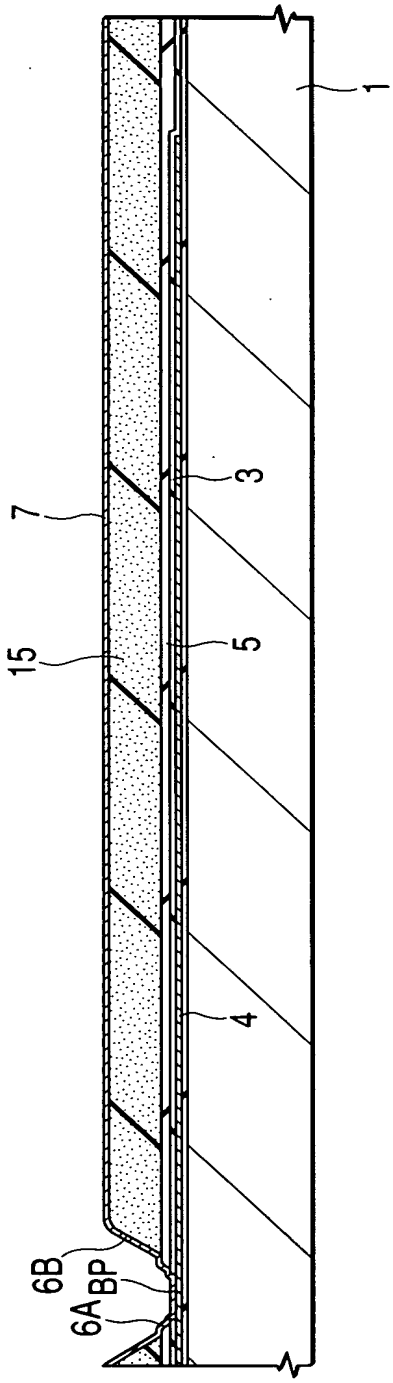


FIG. 31

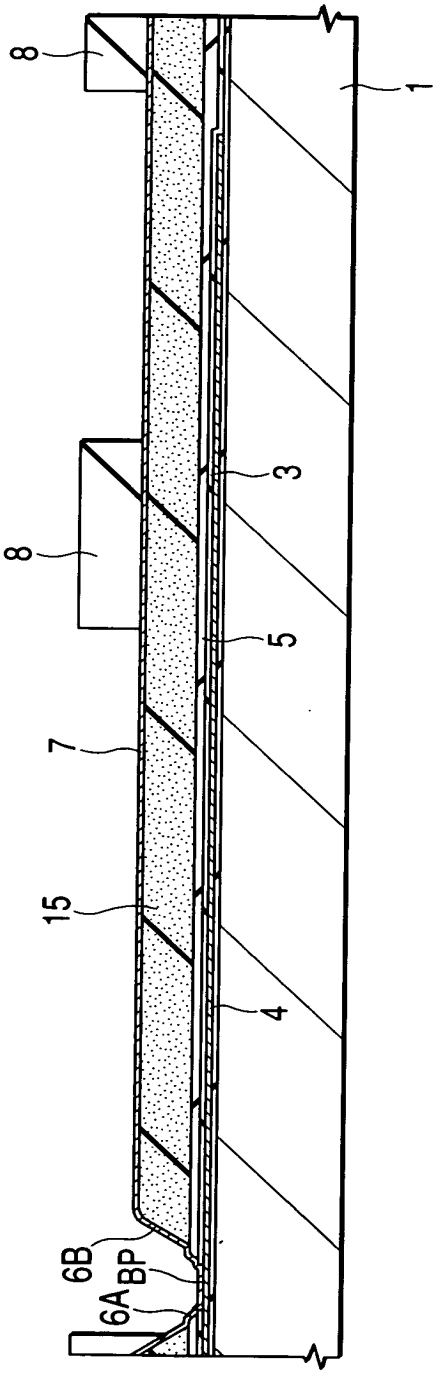


FIG. 32

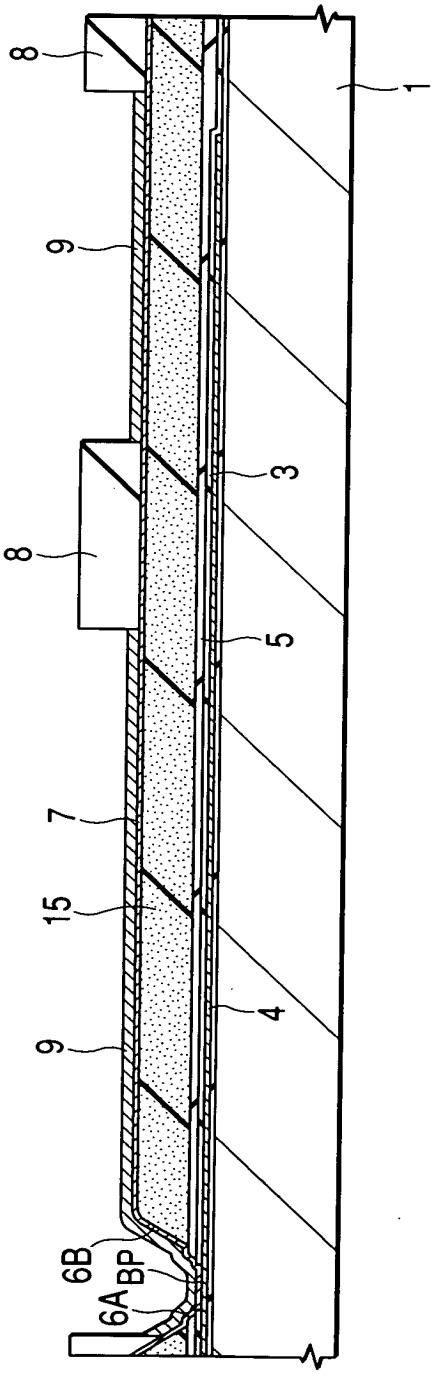


FIG. 33

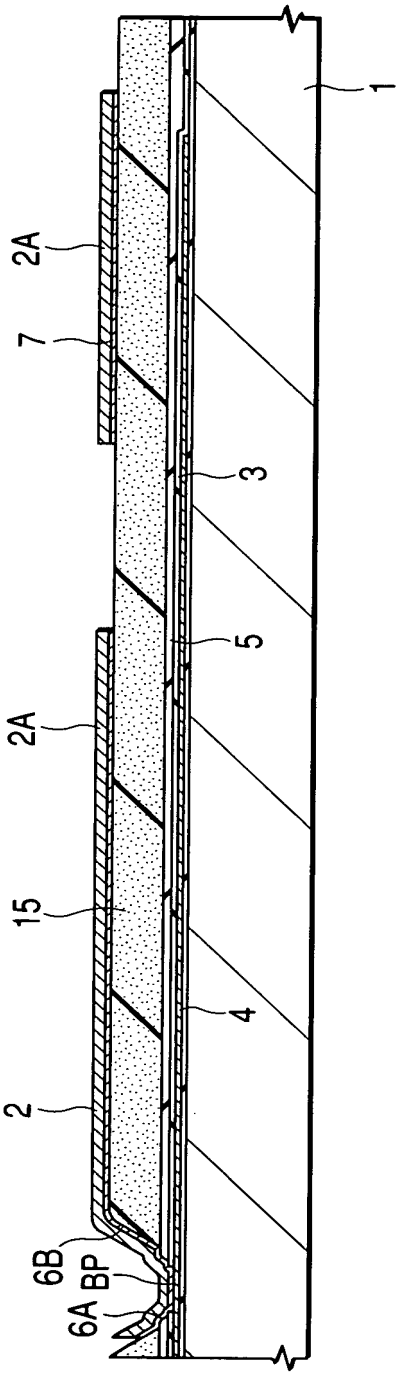


FIG. 34

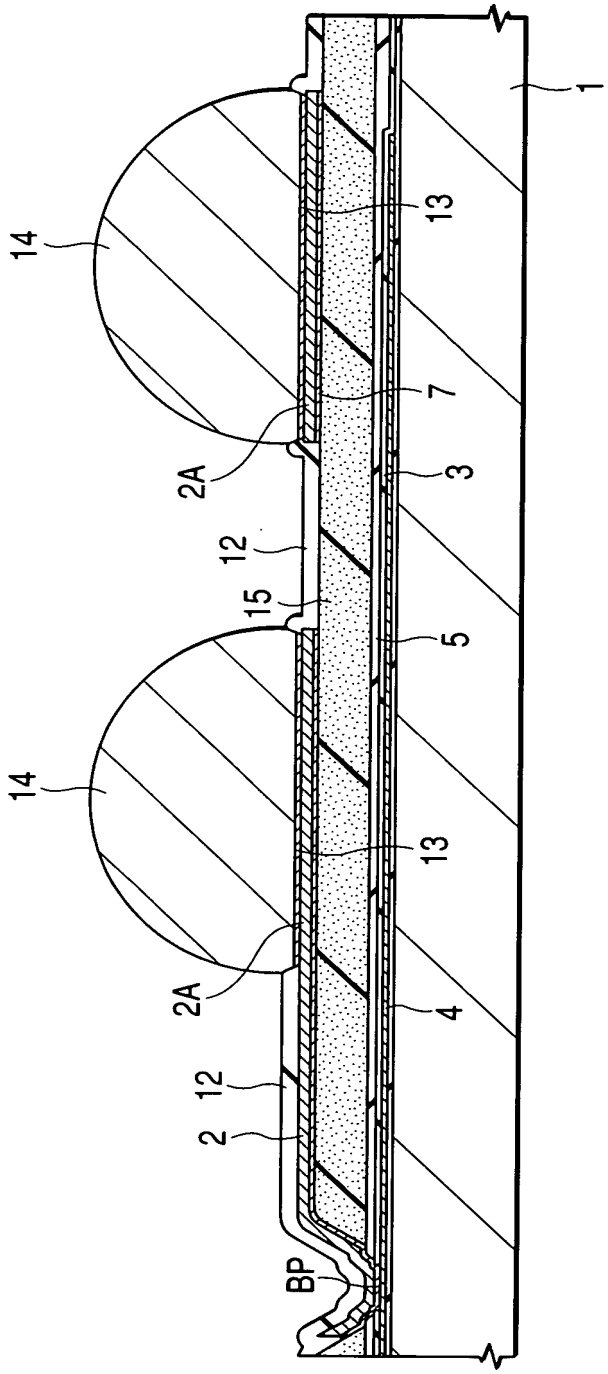
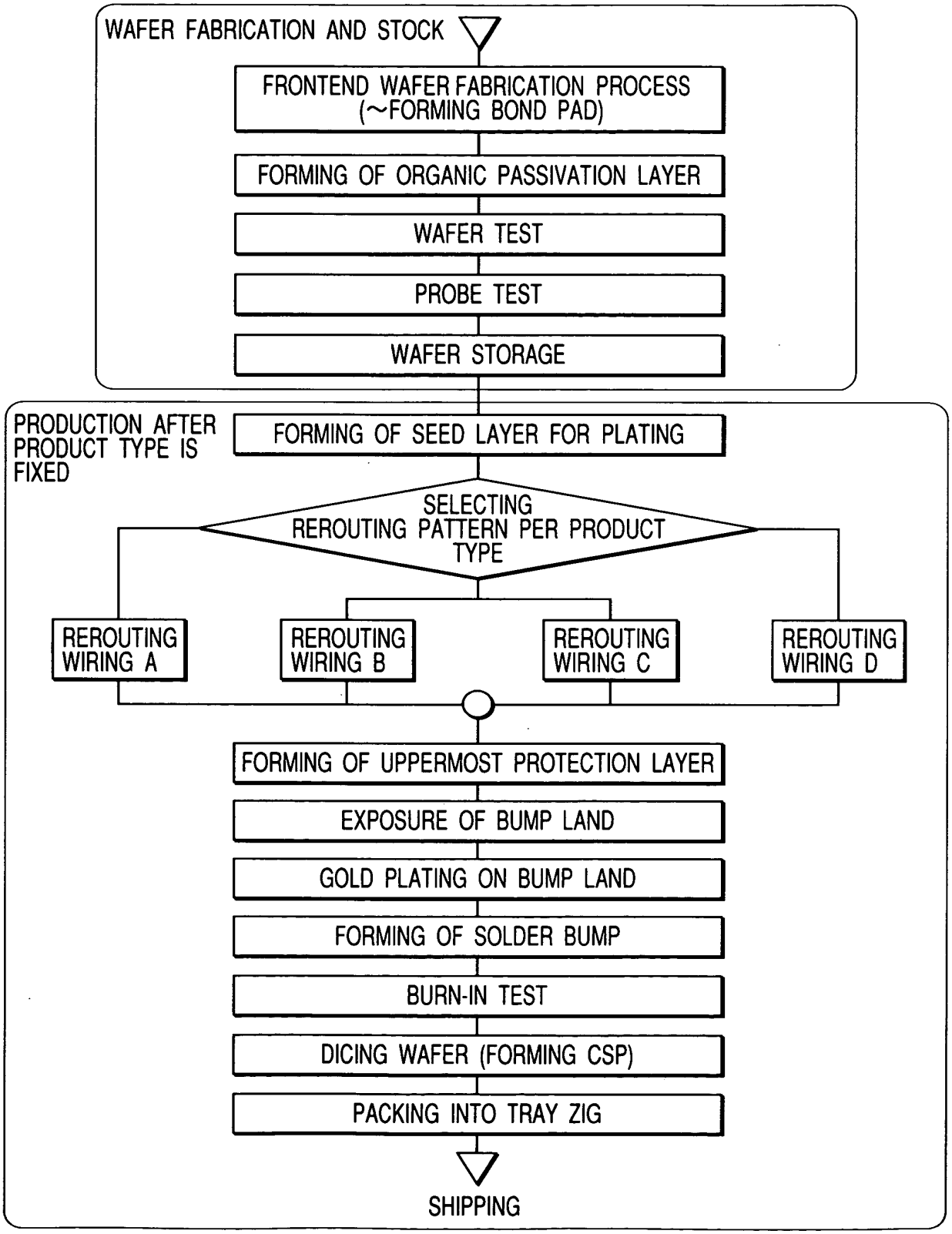


FIG. 35


WAFER FABRICATION AND STOCK
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GOLD PLATING ON BUMP LAND
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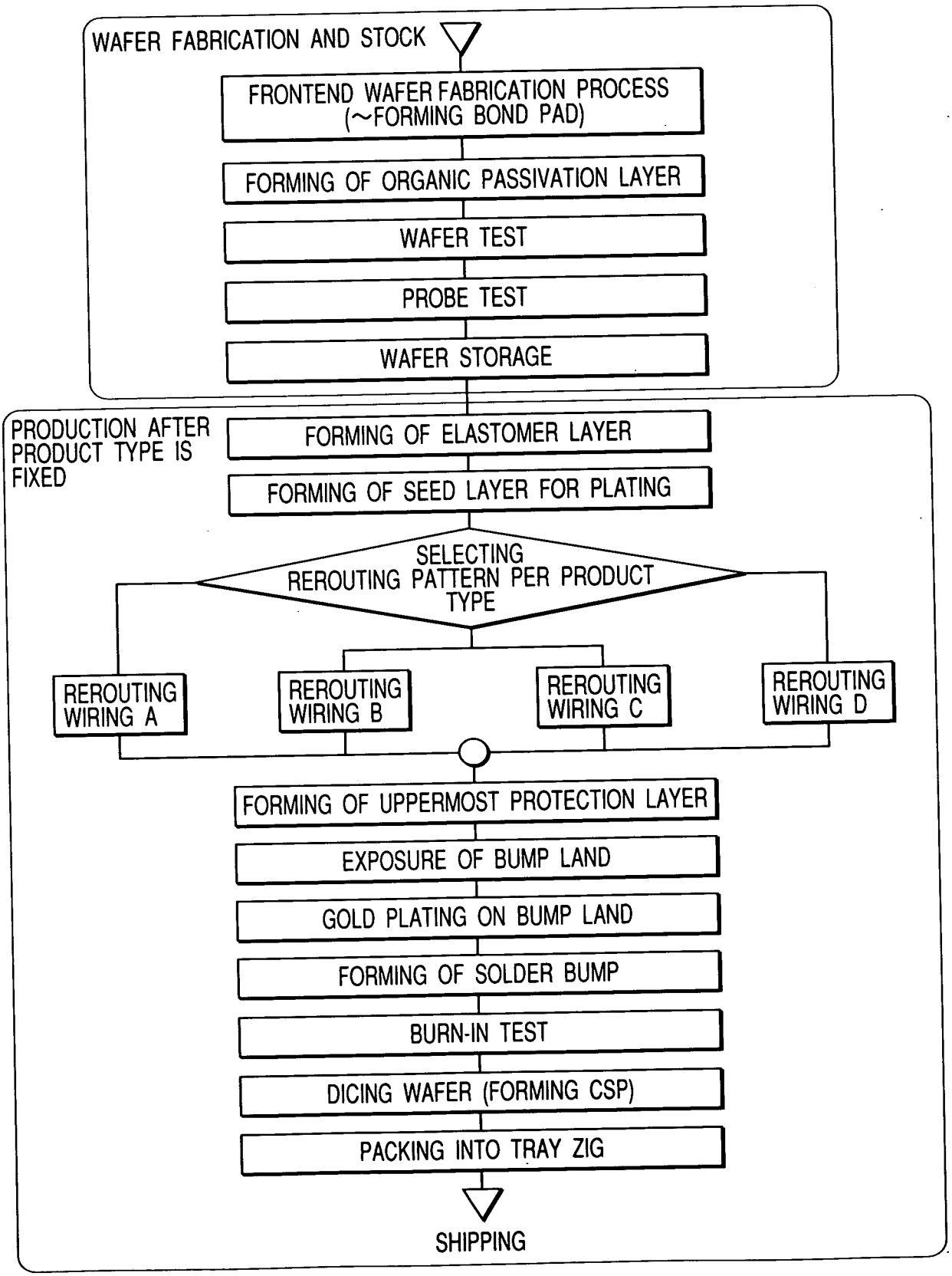
BURN-IN TEST
DICING WAFER (FORMING CSP)
PACKING INTO TRAY ZIG
SHIPPING

FIG. 36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GOLD PLATING ON BUMP LAND
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PACKING INTO TRAY ZIG
SHIPPING

FIG. 37

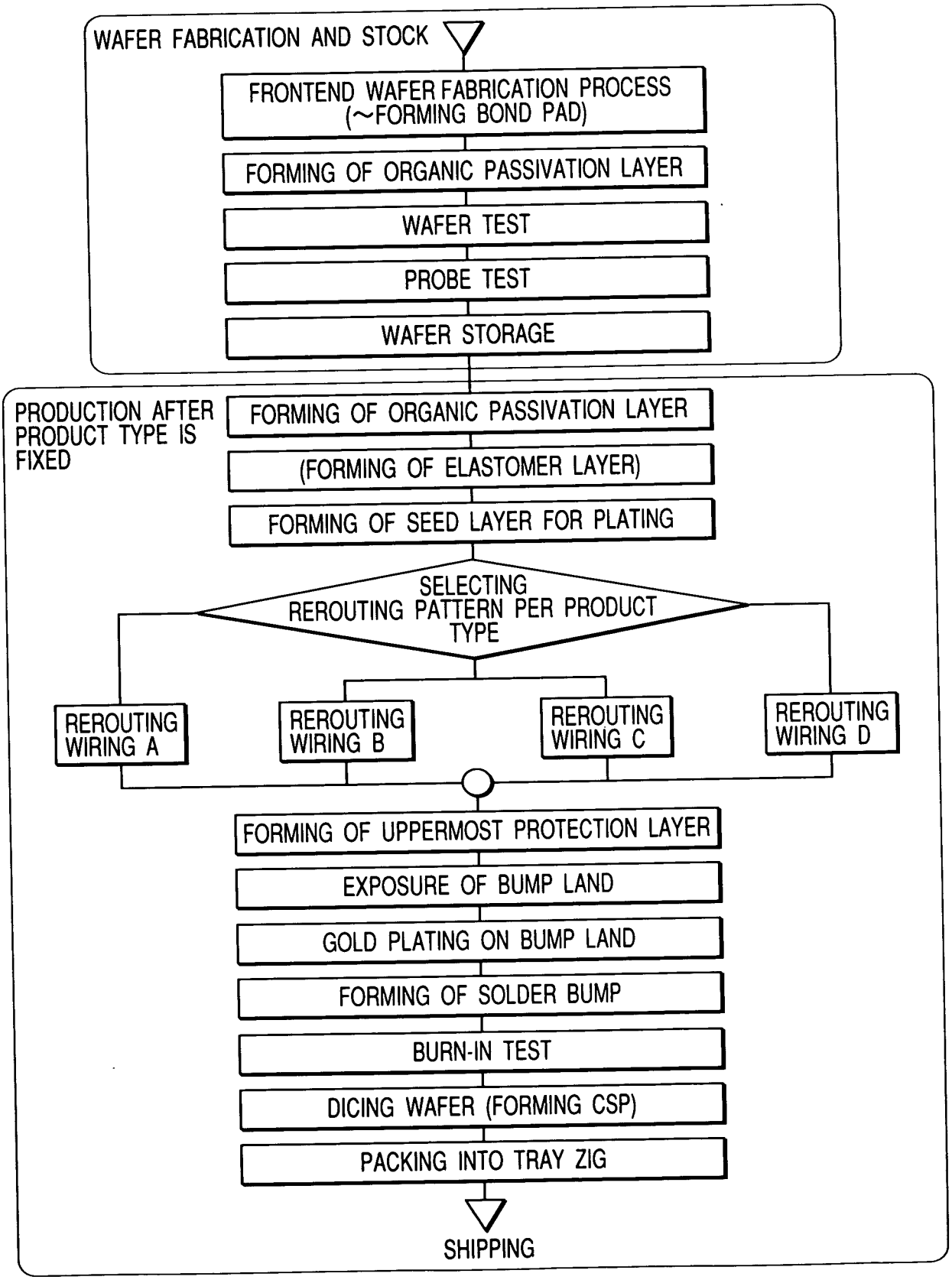
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FIG. 38

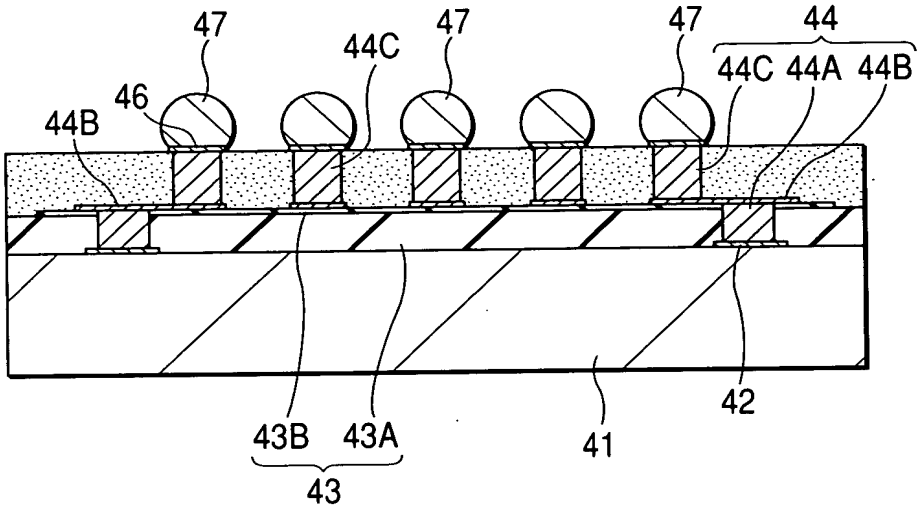


FIG. 39

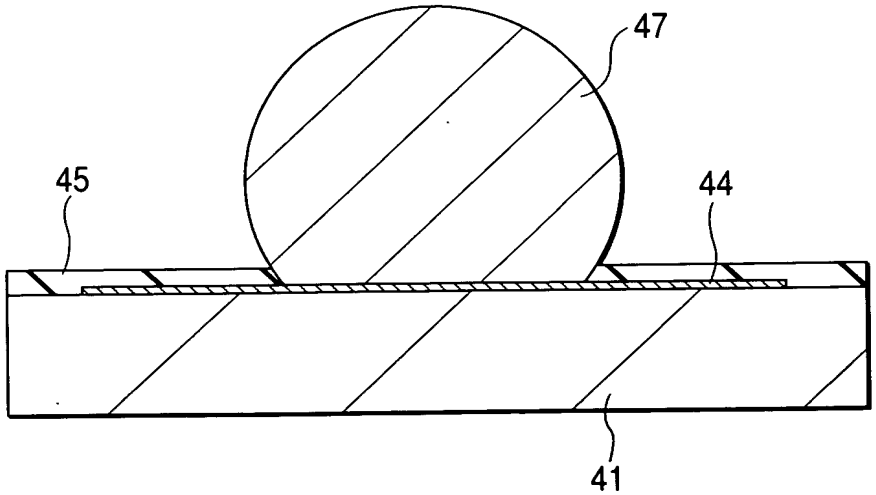


FIG. 40

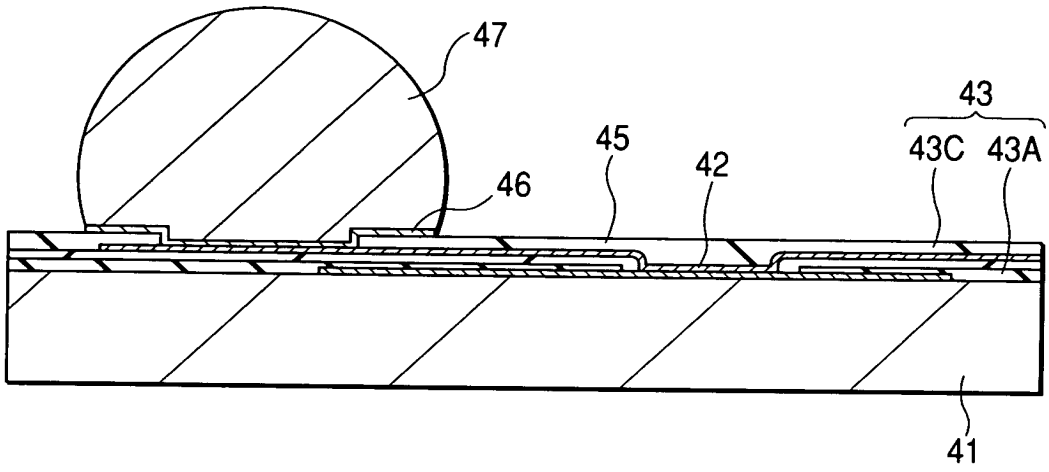


FIG. 41

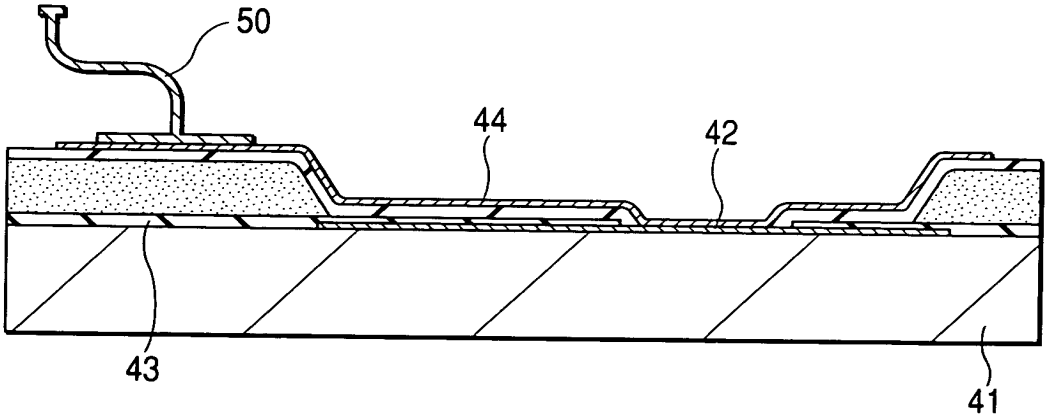
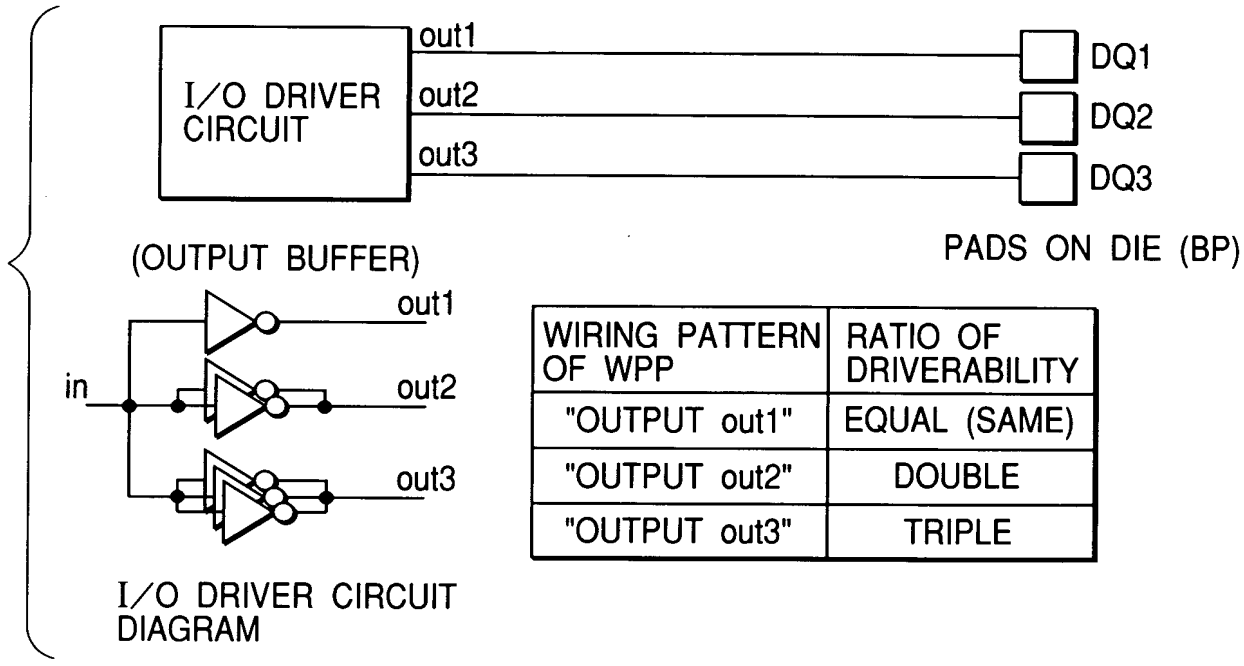


FIG. 42



WIRING PATTERN OF WPP	RATIO OF DRIVERABILITY
"OUTPUT out1"	EQUAL (SAME)
"OUTPUT out2"	DOUBLE
"OUTPUT out3"	TRIPLE

FIG. 43

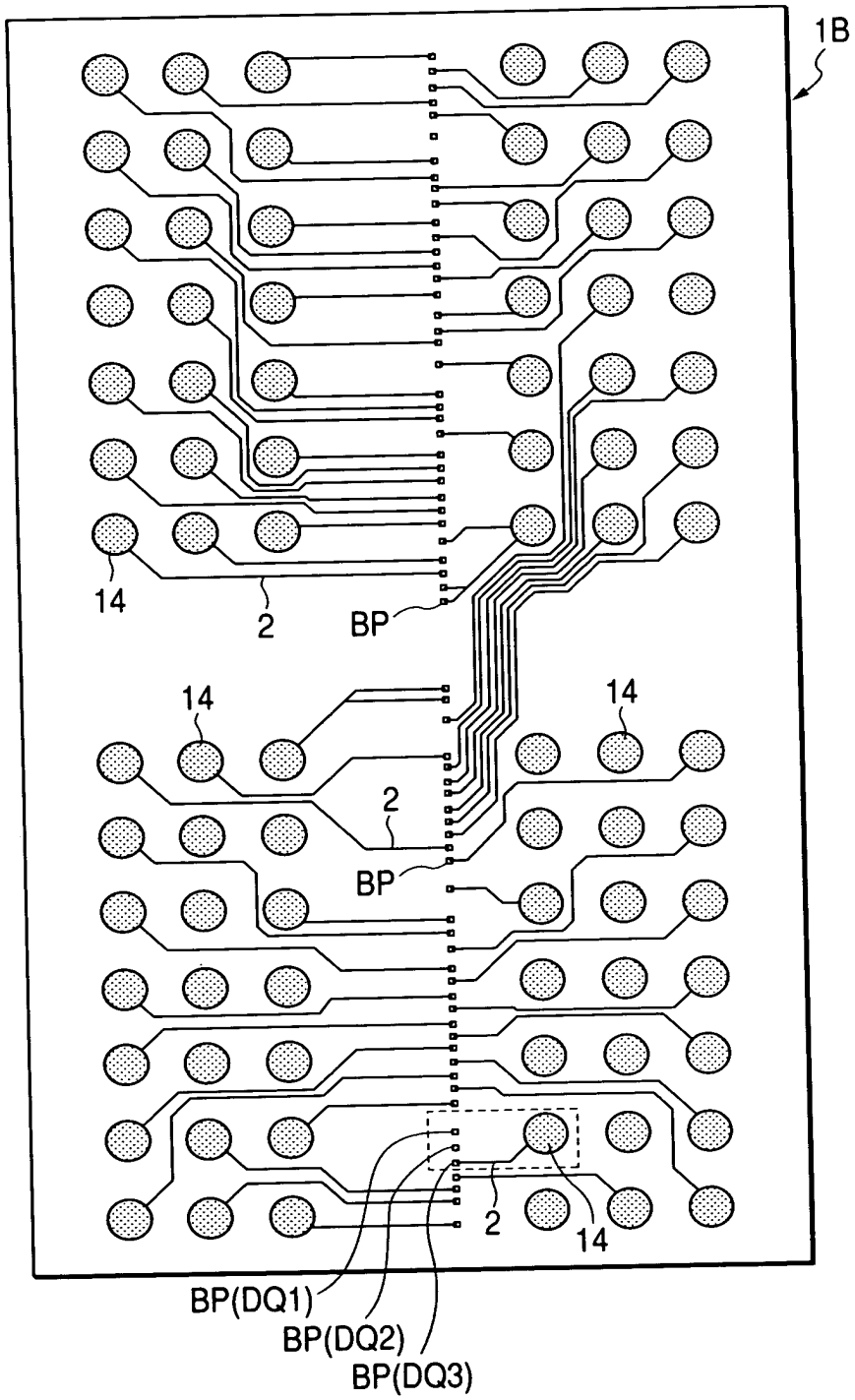


FIG. 44(a)

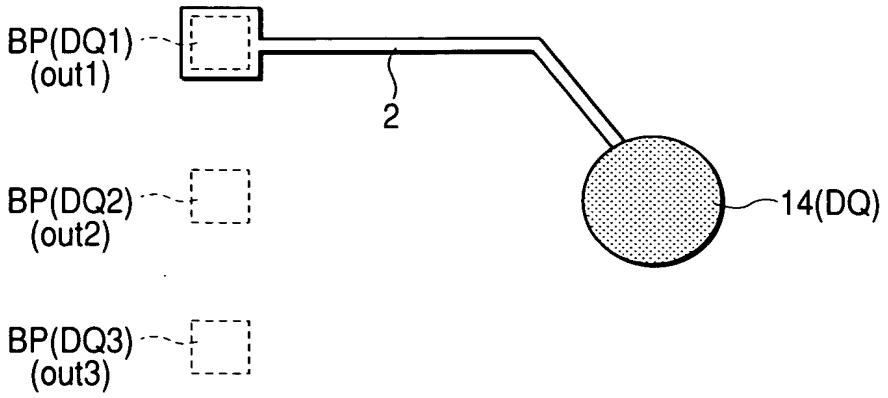


FIG. 44(b)

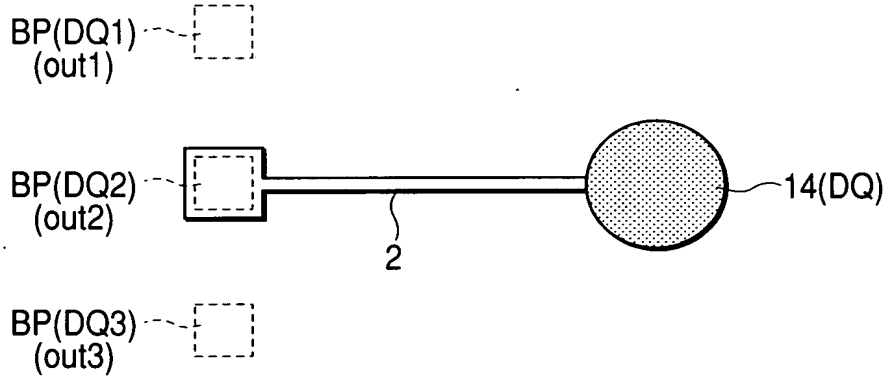


FIG. 44(c)

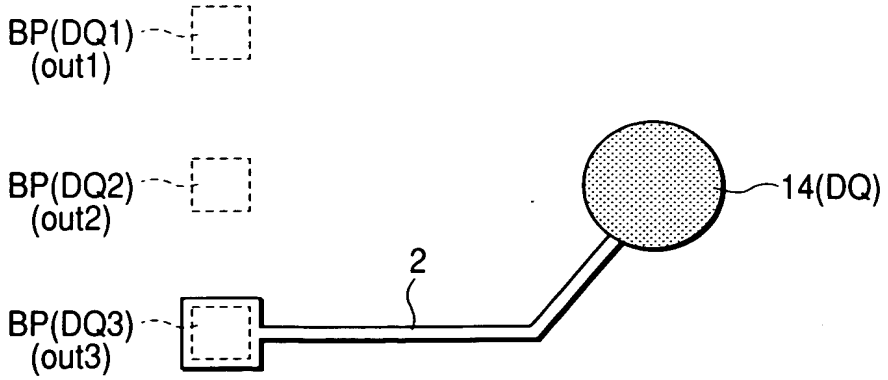


FIG. 45

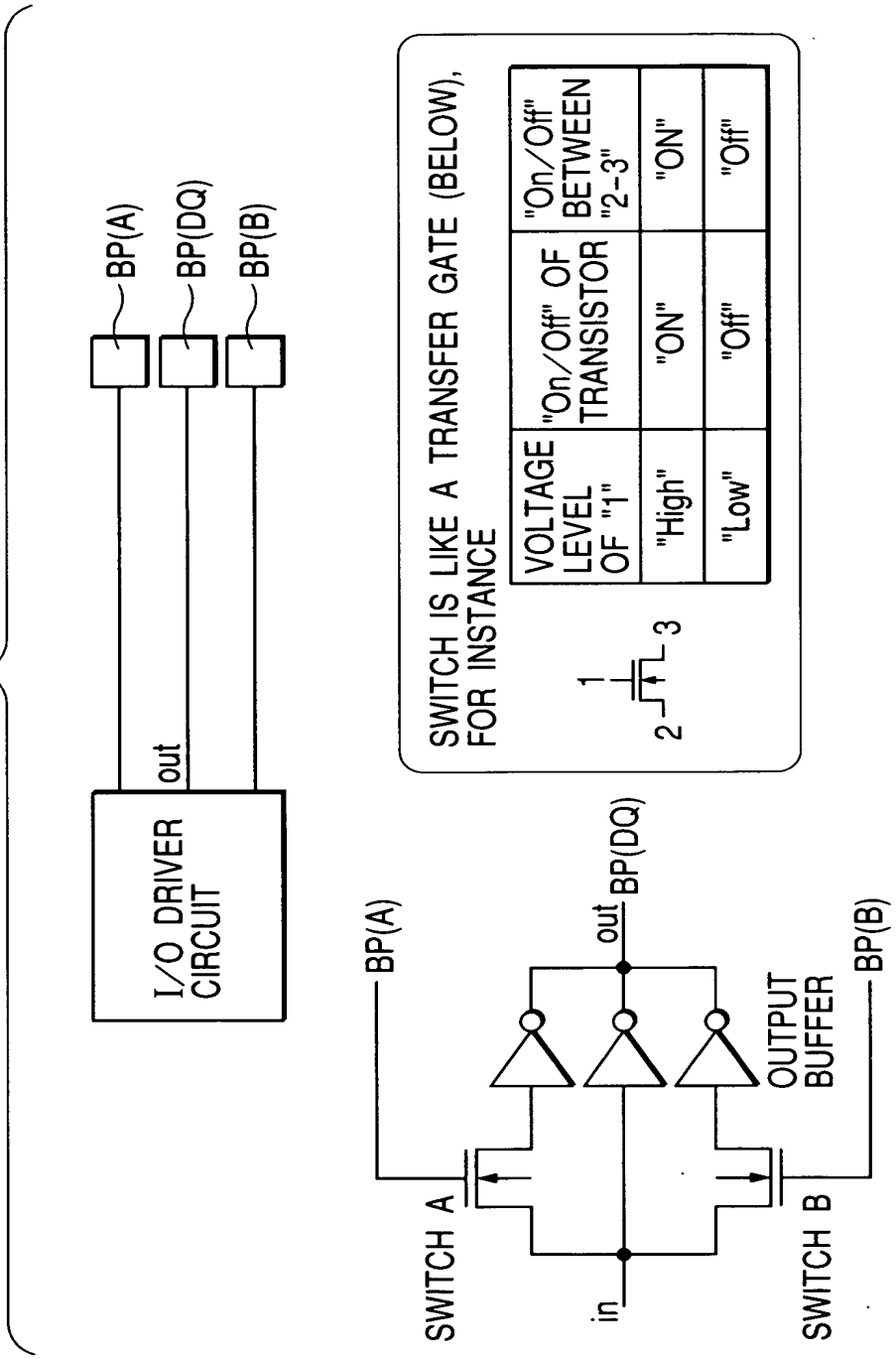

BP(A)
BP(DQ)
BP(B)
out
I/O DRIVER CIRCUIT
SWITCH IS LIKE A TRANSFER GATE (BELOW), FOR INSTANCE
VOLTAGE LEVEL OF "1"
"On/Off" OF TRANSISTOR
"On/Off" BETWEEN "2-3"
"High"
"ON"
"ON"
"Low"
"Off"
"Off"
1
2
3
BP(A)
out
BP(DQ)
SWITCH A
in
OUTPUT BUFFER
SWITCH B
BP(B)

FIG. 46(a)

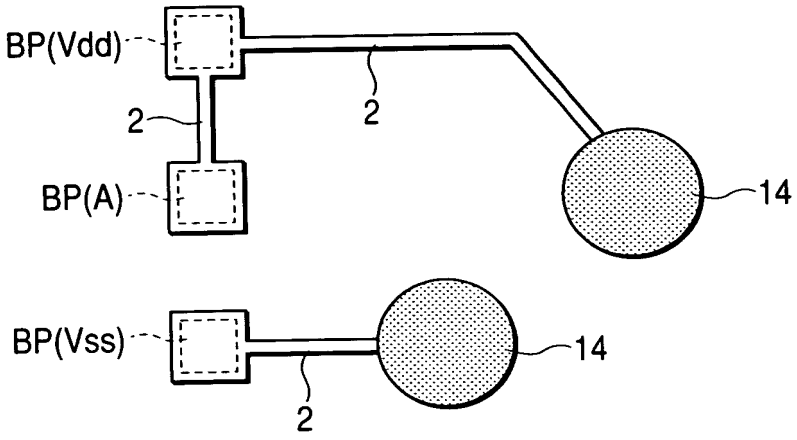


FIG. 46(b)

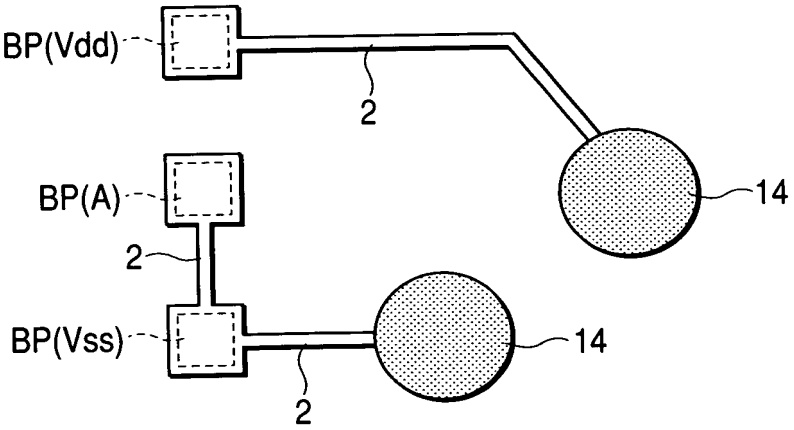


FIG. 46(c)

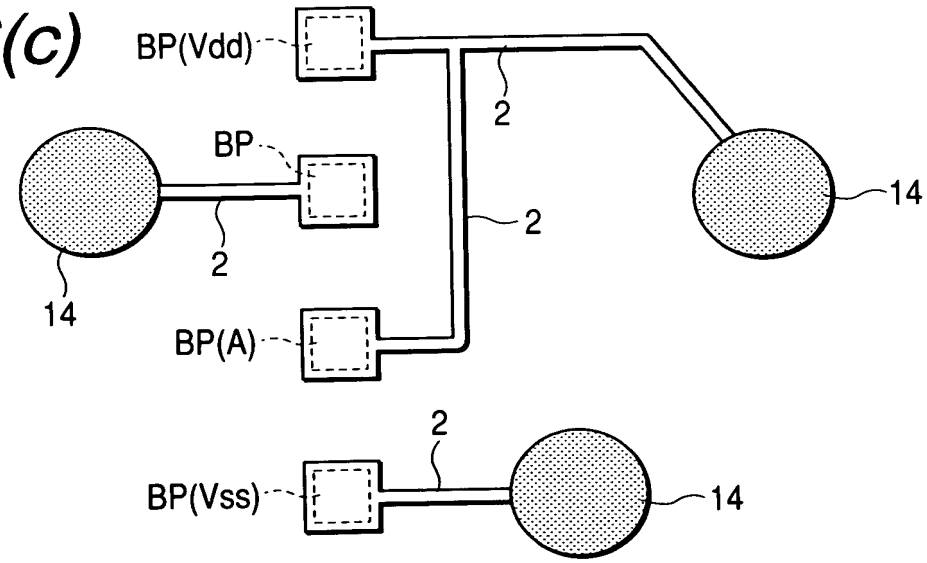
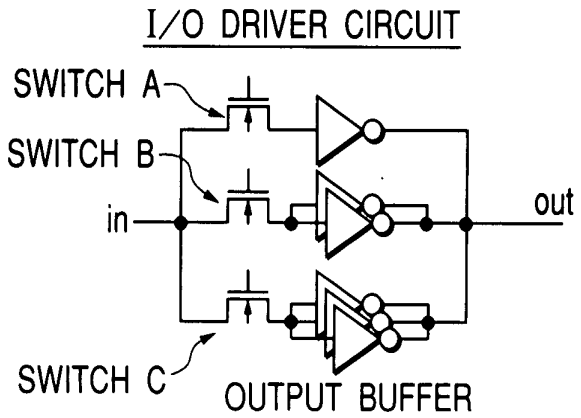
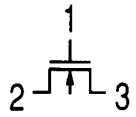


FIG. 47



SWITCH IS LIKE A TRANSFER GATE (BELOW), FOR INSTANCE



VOLTAGE LEVEL OF "1"	"On/Off" OF TRANSISTOR	"On/Off" BETWEEN "2-3"
"High"	"ON"	"ON"
"Low"	"Off"	"Off"

On/Off OF EACH TRANSISTOR (A/B/C)	RATIO OF DRIVERABILITY
"On/Off/Off"	×1
"Off/On/Off"	×2
"Off/Off/On"	×3
"On/Off/On"	×4
"Off/On/On"	×5
"On/On/On"	×6

FIG. 48(a)

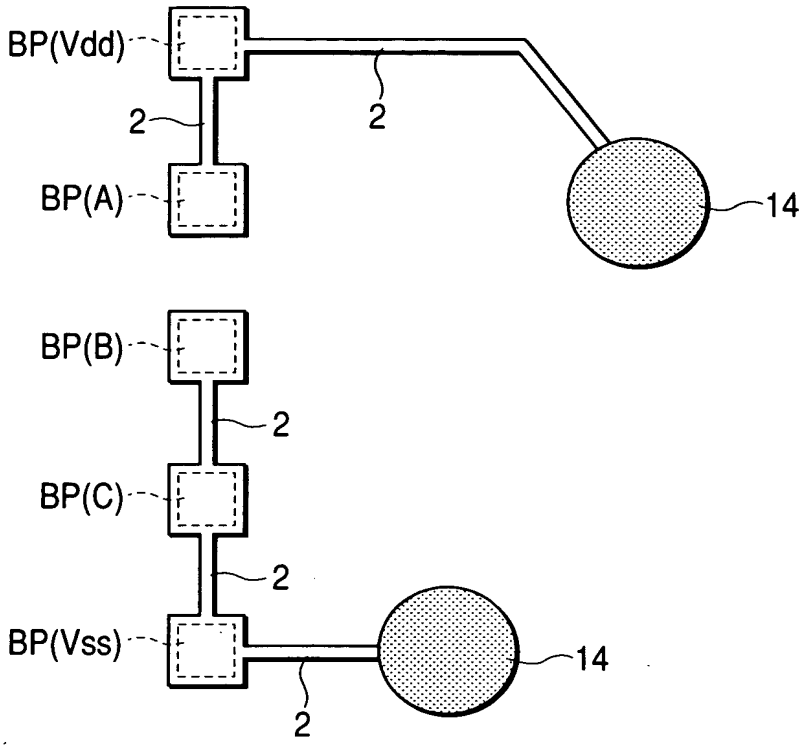


FIG. 48(b)

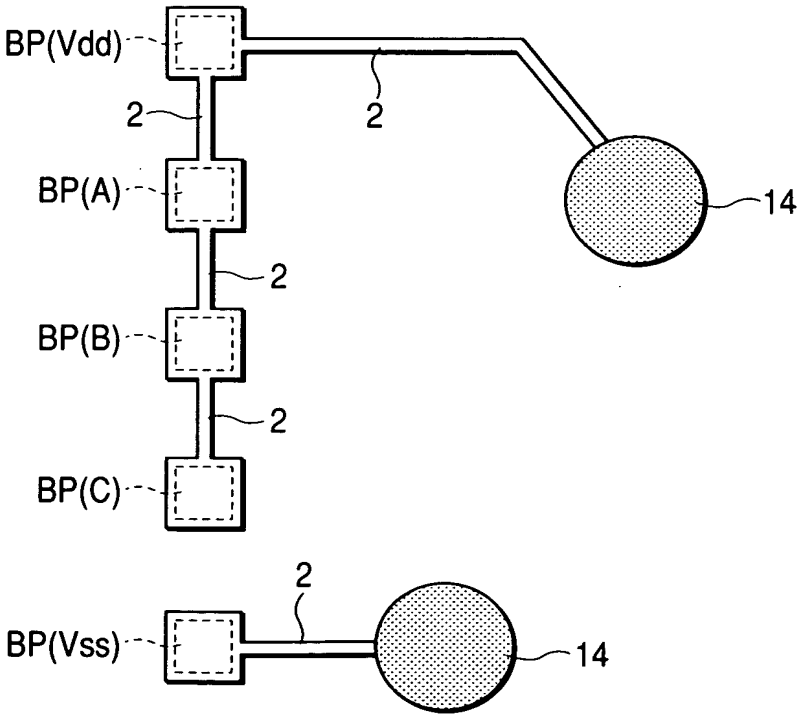
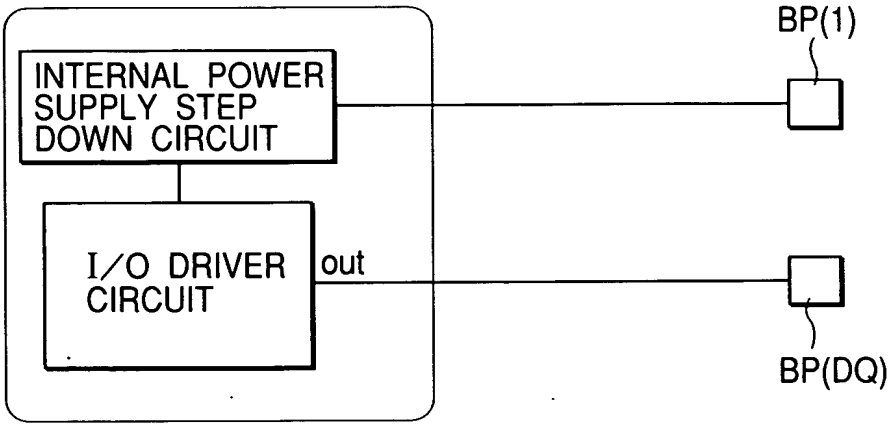
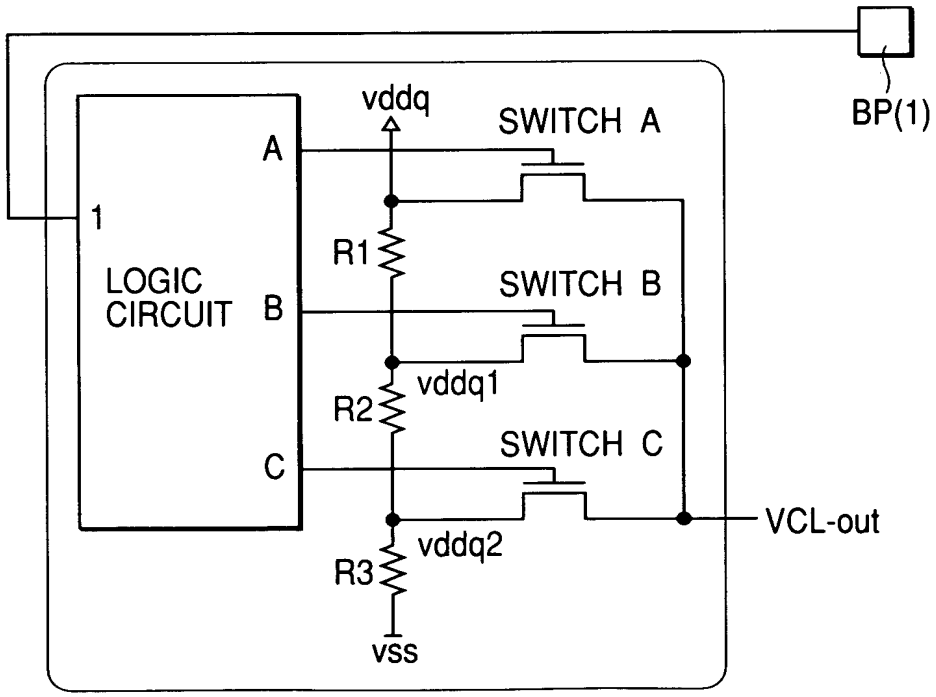


FIG. 49



VARIABLE VOLTAGE AMPLITUDE CIRCUIT FOR I/O BUFFER

FIG. 50



INTERNAL POWER SUPPLY STEP DOWN CIRCUIT

FIG. 51

VOLTAGE LEVEL AT "1"	VOLTAGE LEVEL AT "A/B/C"	"On/Off" OF SWITCH "a/b/c"	VOLTAGE LEVEL AT "VCL-out"
"NO INPUT"	"High/Low/Low"	"On/Off/Off"	"vddq"
"High"	"Low/High/Low"	"Off/On/Off"	"vddq1"
"Low"	"Low/Low/High"	"Off/Off/On"	"vddq2"

FIG. 52

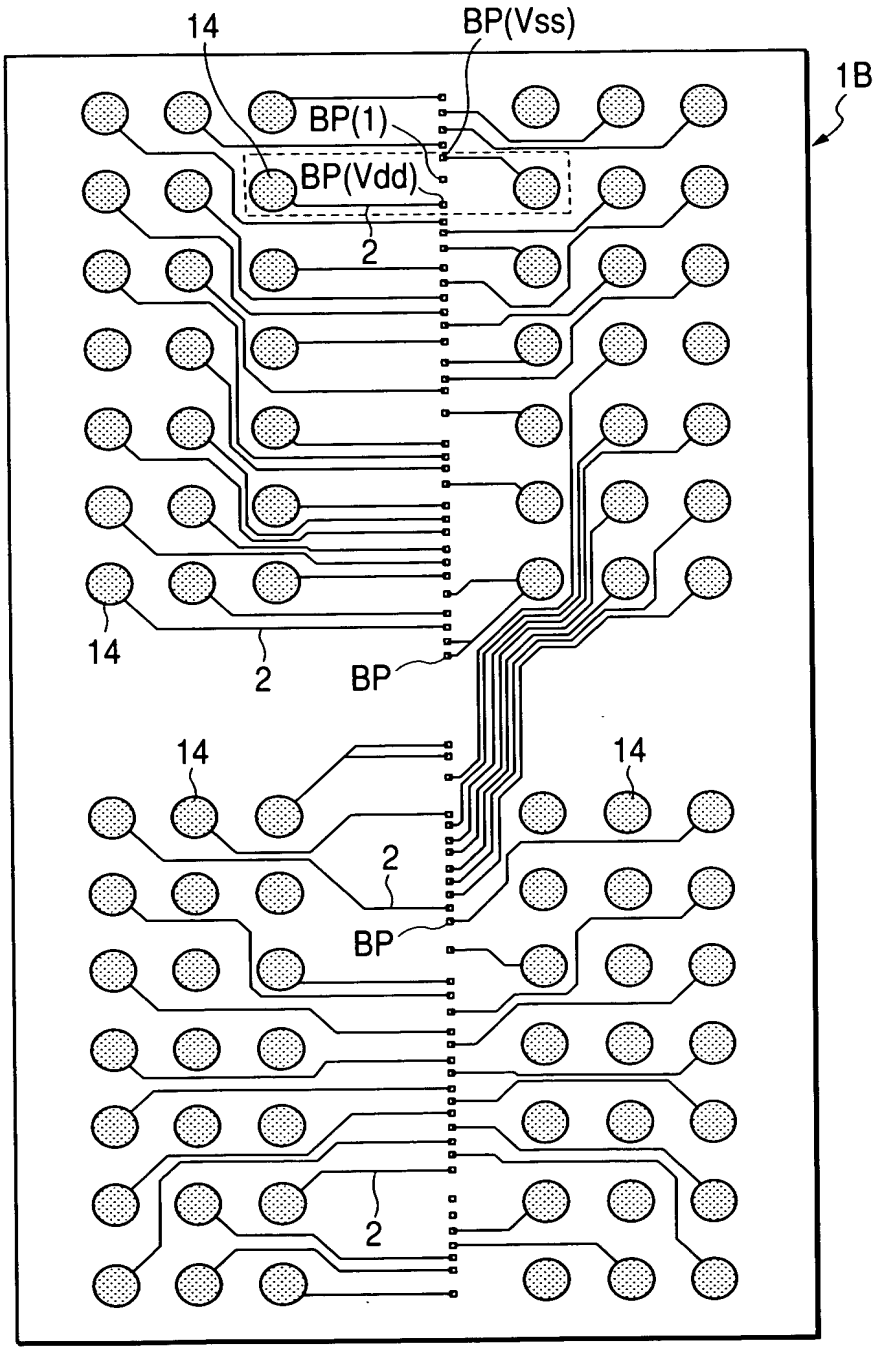


FIG. 53(a)

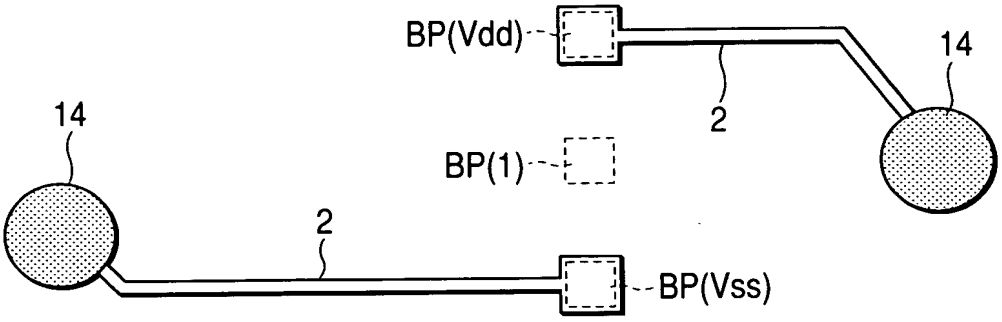


FIG. 53(b)

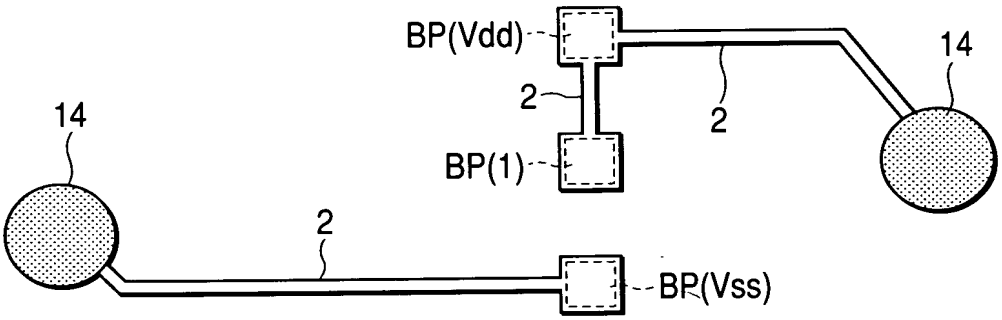


FIG. 53(c)

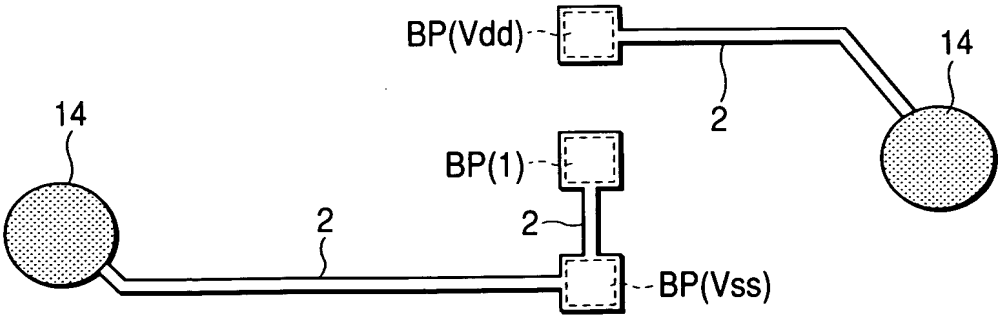


FIG. 54

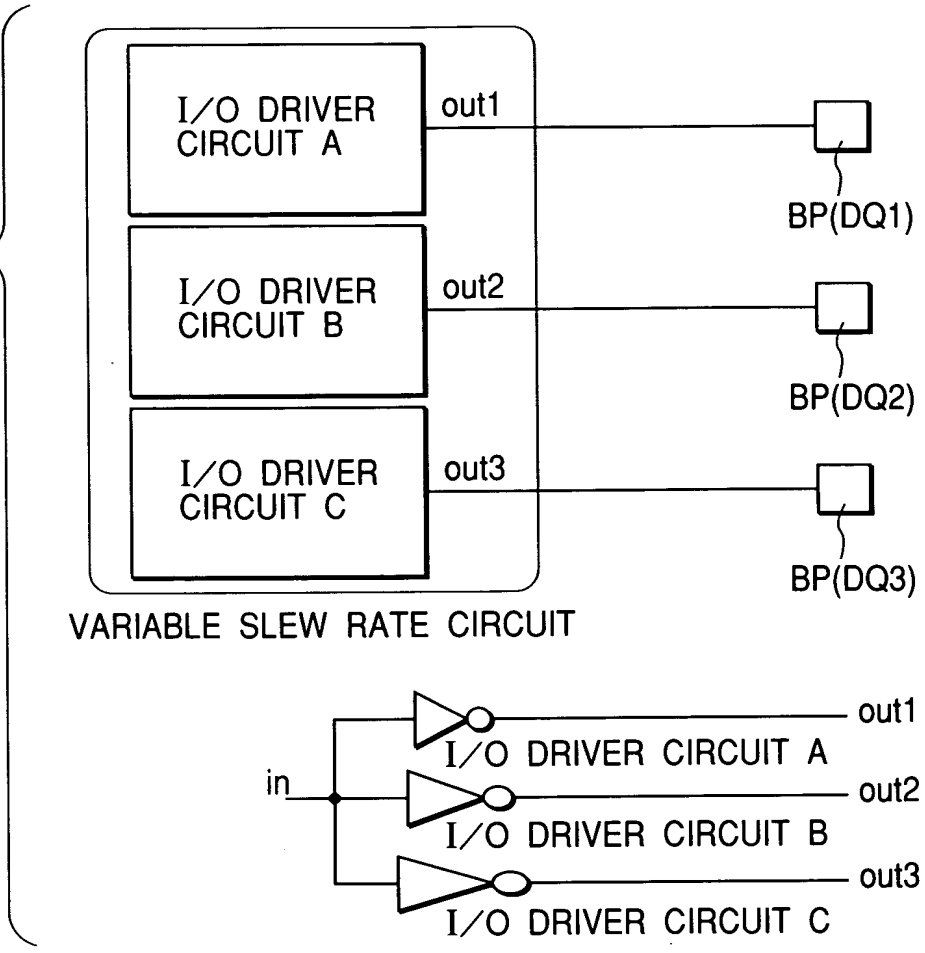

I/O DRIVER CIRCUIT A
I/O DRIVER CIRCUIT B
I/O DRIVER CIRCUIT C
out1
out2
out3
BP(DQ1)
BP(DQ2)
BP(DQ3)
VARIABLE SLEW RATE CIRCUIT
in
out1
out2
out3
I/O DRIVER CIRCUIT A
I/O DRIVER CIRCUIT B
I/O DRIVER CIRCUIT C

FIG. 55

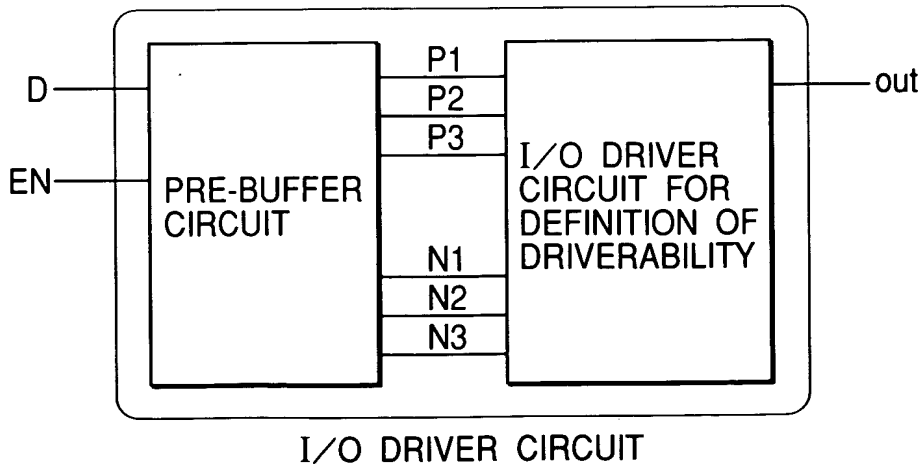

D
EN
PRE-BUFFER CIRCUIT
P1
P2
P3
N1
N2
N3
I/O DRIVER CIRCUIT FOR DEFINITION OF DRIVERABILITY
out
I/O DRIVER CIRCUIT

FIG. 56

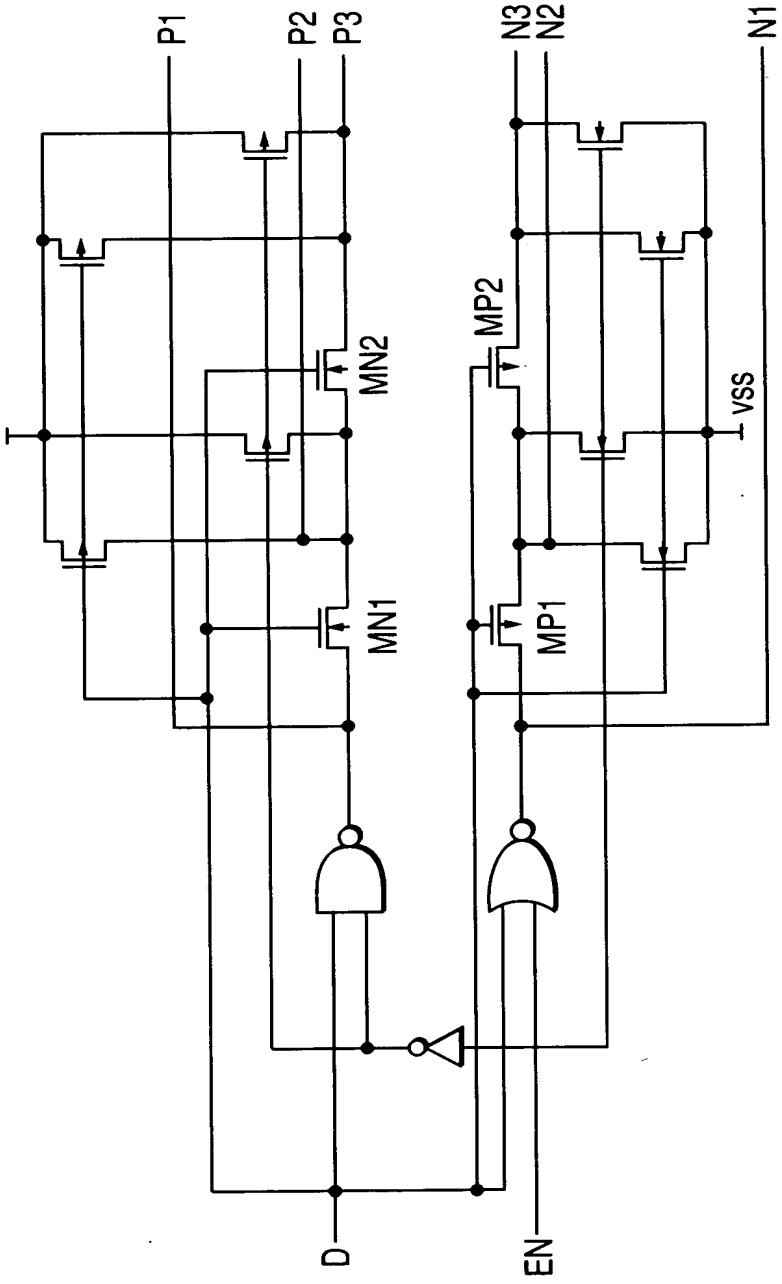
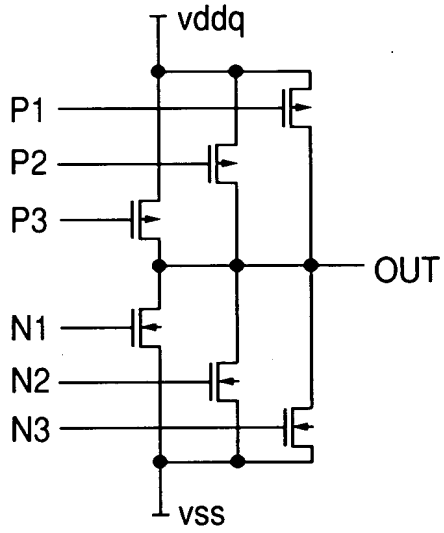


FIG. 57



I/O DRIVER CIRCUIT FOR
DEFINITION OF DRIVERABILITY

FIG. 58

W/L RATIO OF MP1 AND MP2	W/L RATIO OF MN1 AND MN2	SLEW RATE
5/1	5/2	×1 (I/O DRIVER CIRCUIT A)
5/2	5/4	×2 (I/O DRIVER CIRCUIT B)
5/3	5/6	×3 (I/O DRIVER CIRCUIT C)

THE BIGGER THE SLEW RATE IS THE SMOOTHER THE WAVE FORM.

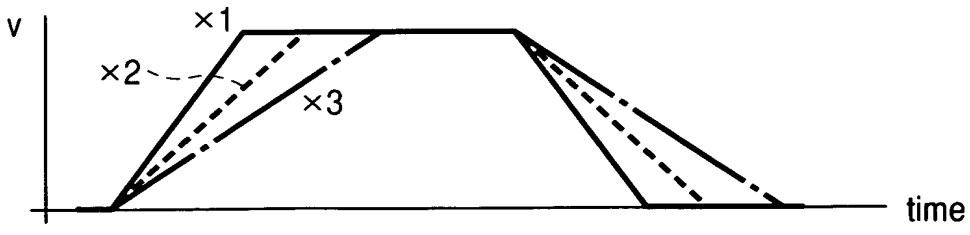


FIG. 59

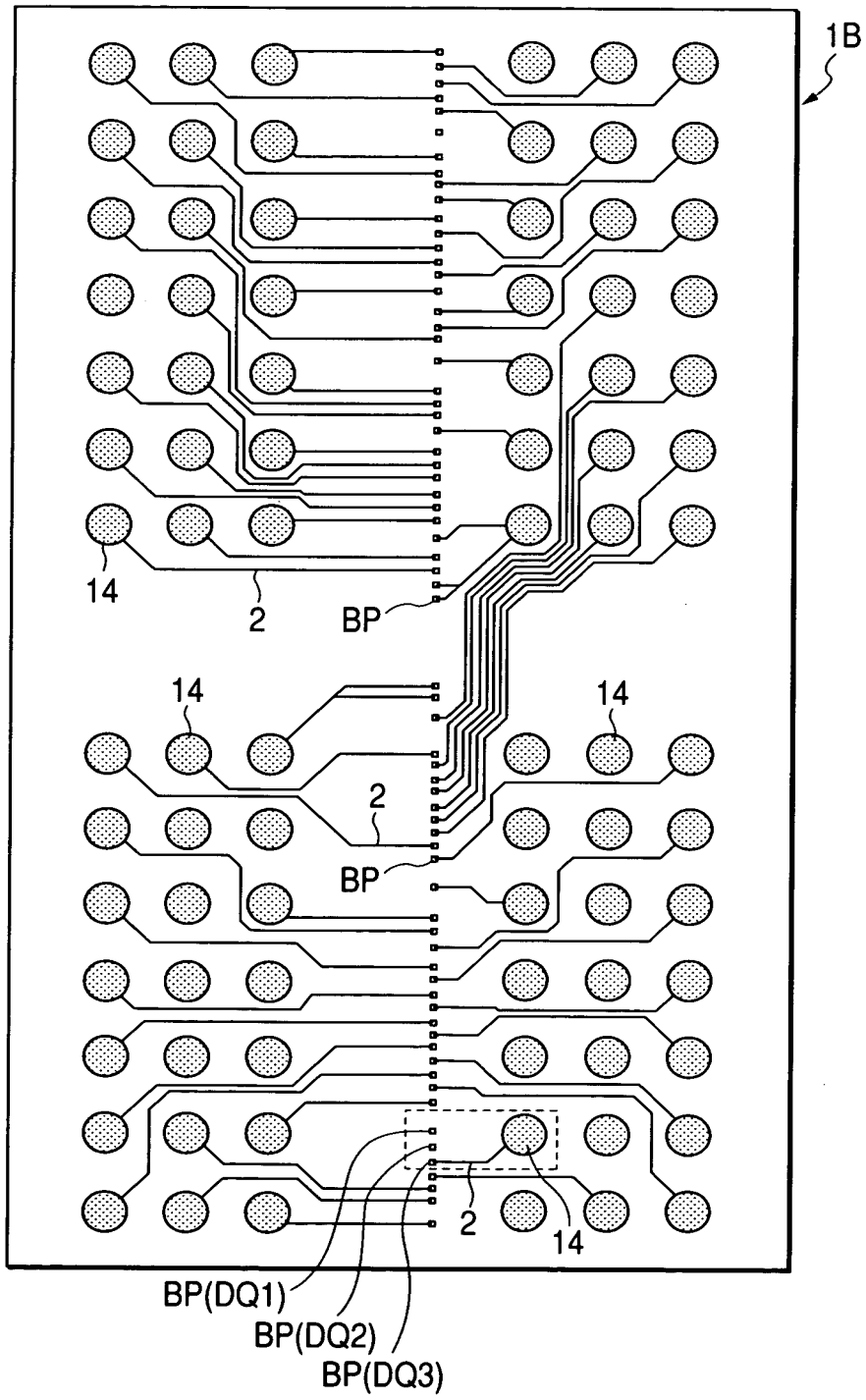


FIG. 60(a)

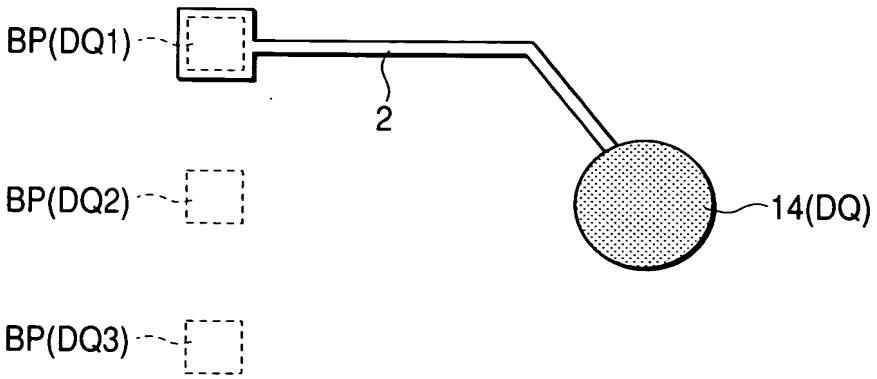


FIG. 60(b)

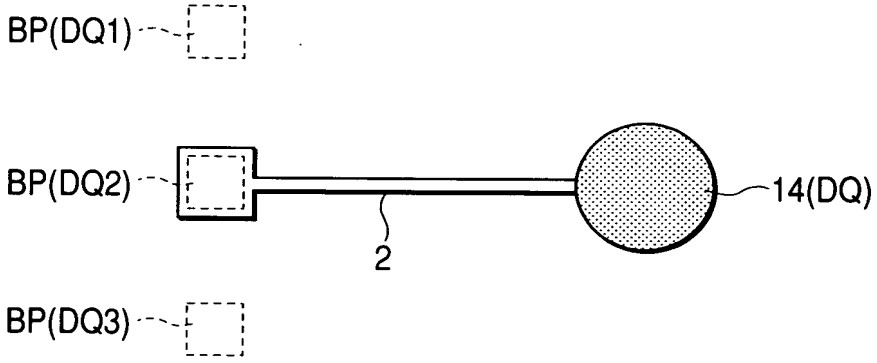


FIG. 60(c)

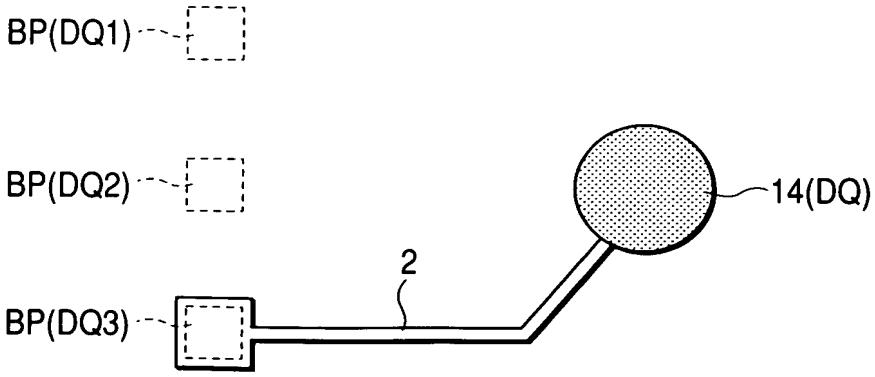
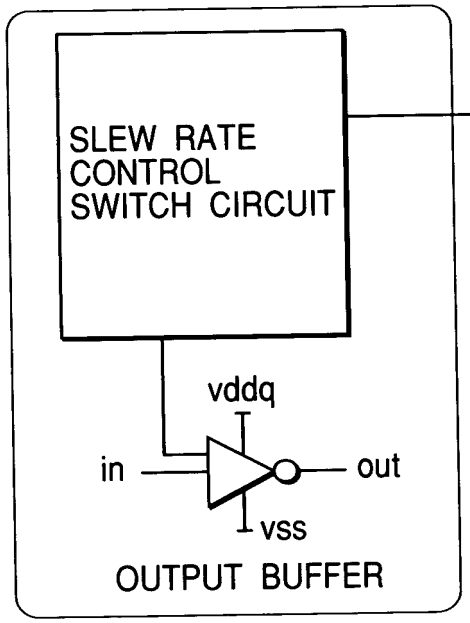


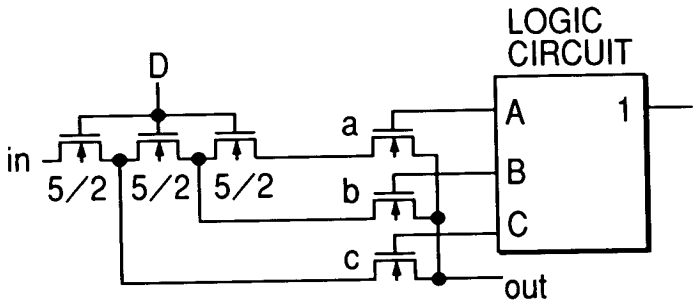
FIG. 61



VOLTAGE LEVEL AT "1"	SLEW RATE
"NO INPUT"	×1
"High"	×2
"Low"	×3

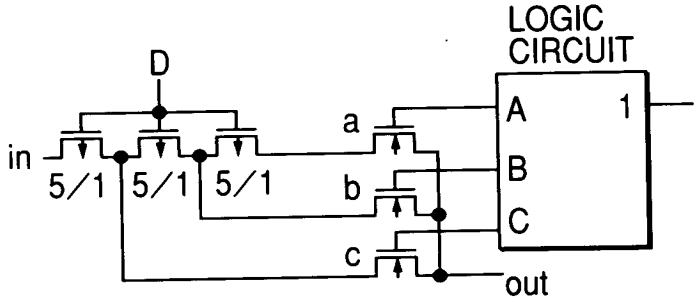
VARIABLE SLEW RATE CIRCUIT

FIG. 62(a)



SLEW RATE CONTROL SWITCH CIRCUIT

FIG. 62(b)



SLEW RATE CONTROL SWITCH CIRCUIT

FIG. 63

LOGIC DIAGRAM FOR LOGIC CIRCUIT (TABLE)

VOLTAGE LEVEL OF "1"	VOLTAGE LEVEL AT "A/B/C"	"On/Off" OF SWITCH "a/b/c"	SLEW RATE
"NO INPUT"	"High/Low/Low"	"On/Off/Off"	×1 (I/O DRIVER CIRCUIT A)
"High"	"Low/High/Low"	"Off/On/Off"	×2 (I/O DRIVER CIRCUIT B)
"Low"	"Low/Low/High"	"Off/Off/On"	×3 (I/O DRIVER CIRCUIT C)

THE BIGGER THE SLEW RATE IS THE SMOOTHER THE WAVE FORM.

FIG. 64(a)

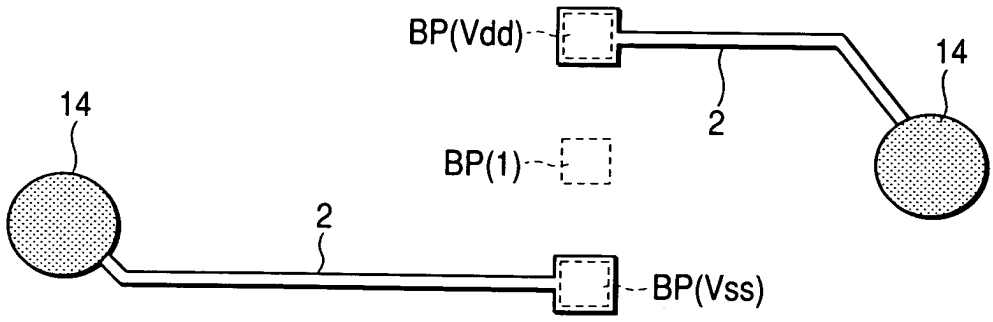


FIG. 64(b)

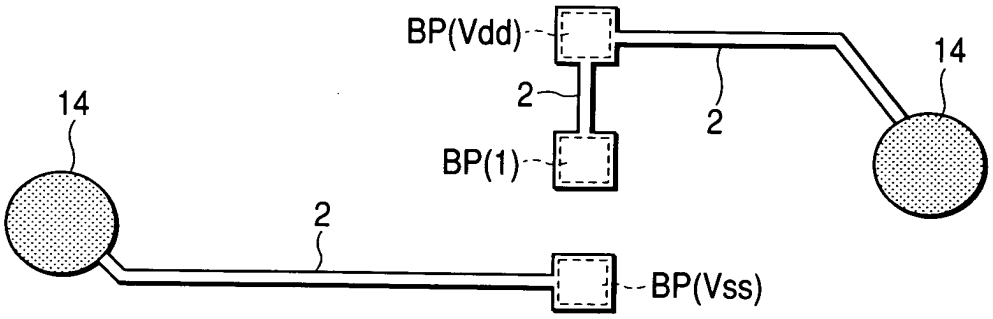


FIG. 64(c)